EE 505

Lecture 26

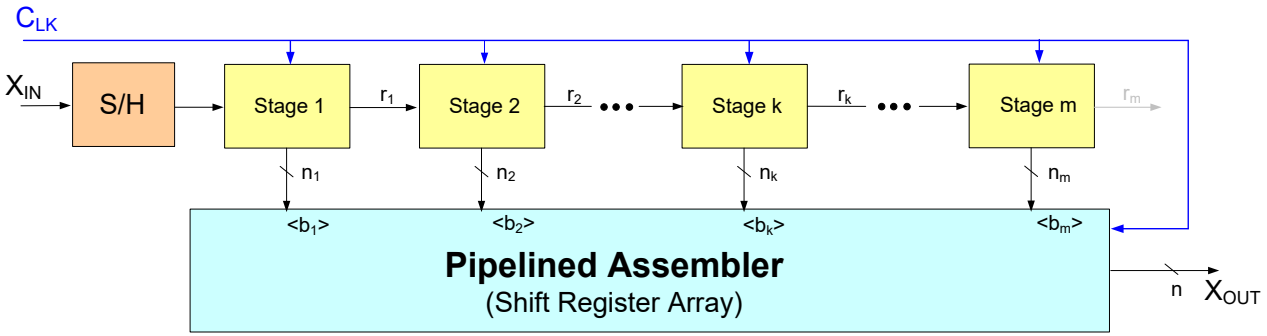
ADC Design
- Pipeline
  - Aperture Uncertainty
  - Cyclic Architectures
  - Eliminating input S/H

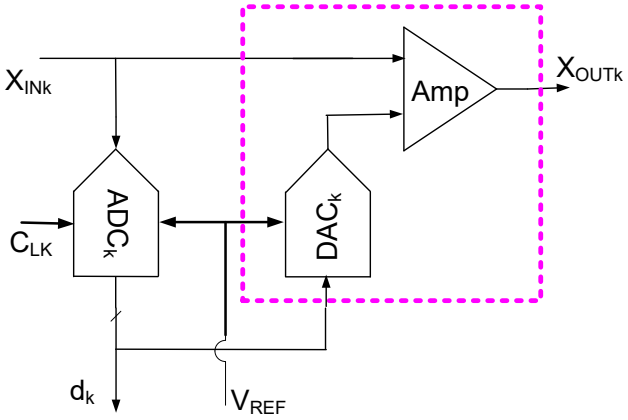
SAR ADC Design

Time Interleaved ADCs

Bootstrapped Switches

Power Dissipation

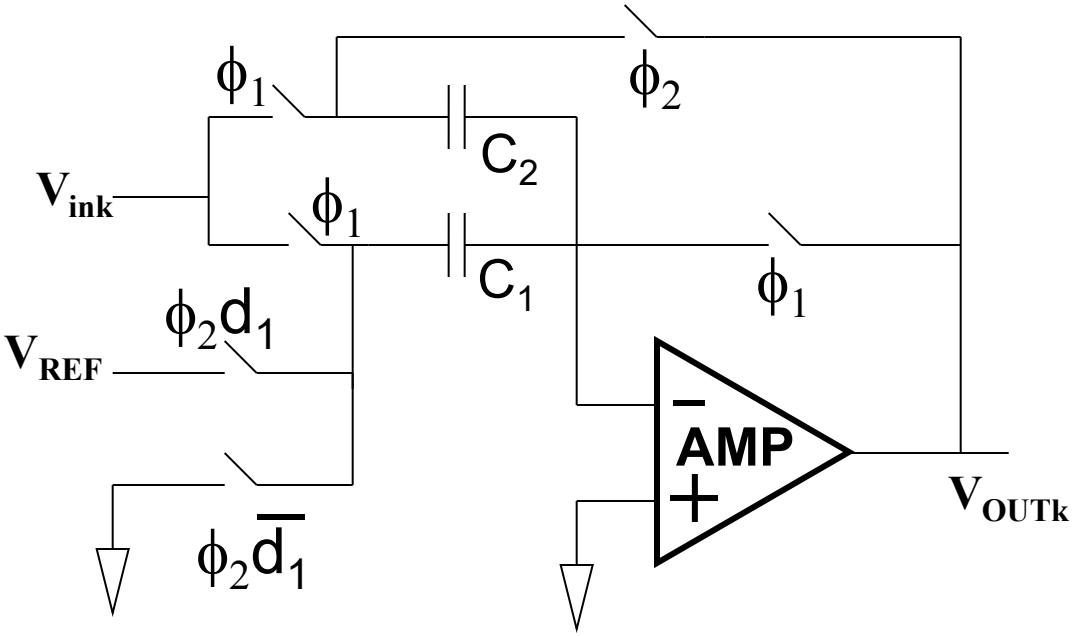




Dominant source of power dissipation is in the op amps in S/H and individual stages

Interstage Amplifiers

Typical Finite-Gain Inter-stage Amplifier
(shown single-ended with 1-bit/stage)



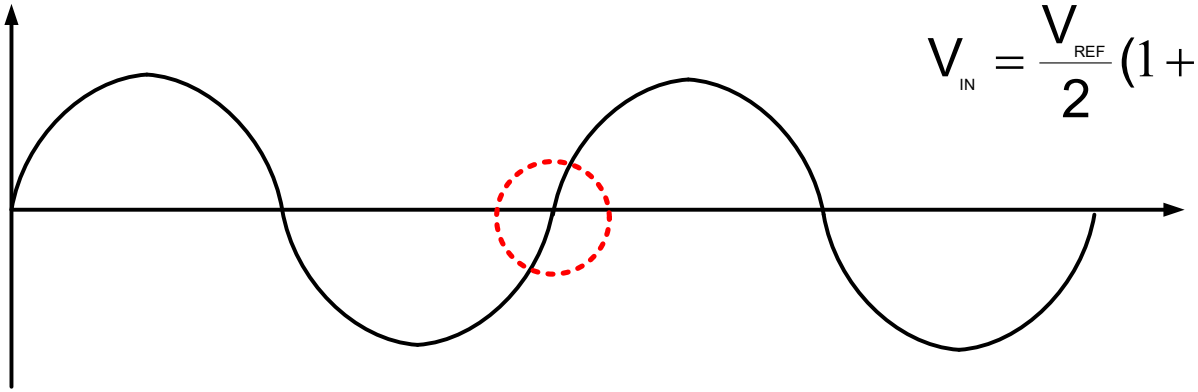
Ideally

$$V_{OUT} = V_{IN}\left(1+\frac{C_1}{C_2}\right) - d_1\left(\frac{C_1}{C_2}\right)V_{REF}$$

$$V_{OUT} = 2V_{IN} - d_1 V_{REF}$$

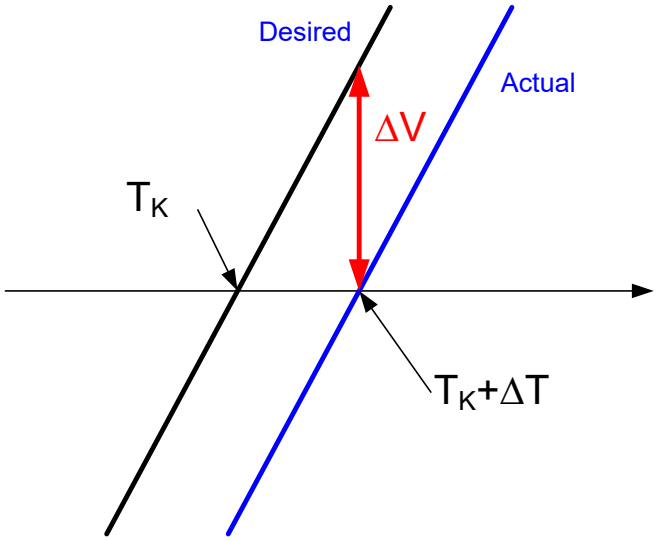
Gain =2.00000

Aperture Uncertainty



$$V_{IN} = \frac{V_{REF}}{2}(1 + \sin\omega t)$$

Aperture Uncertainty: Worst case variation in t that causes ½ LSB error in output



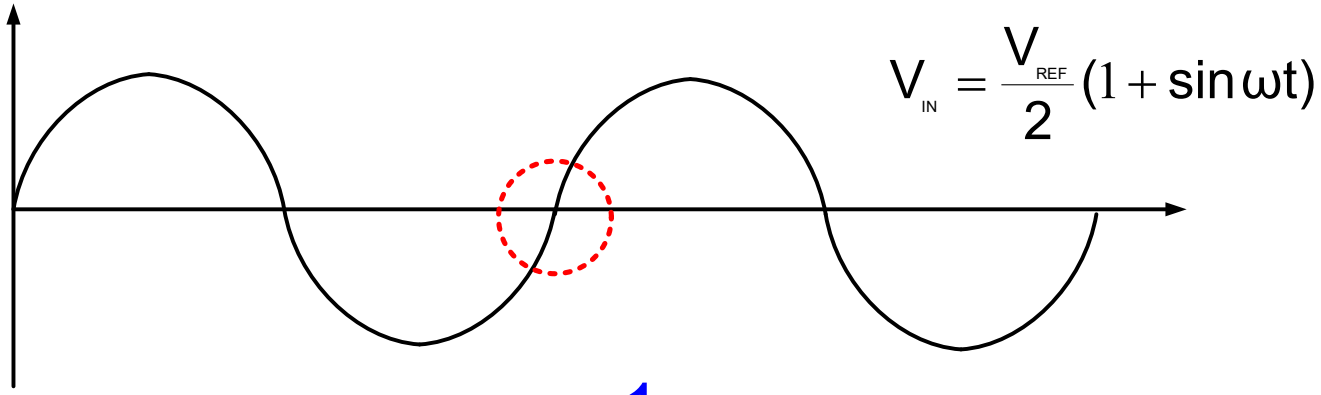
$$\frac{\partial V_{IN}}{\partial t} = \frac{V_{REF}}{2}\omega\cos\omega t)$$

$$\left.\frac{\partial V_{IN}}{\partial t}\right|_{MAX} = \frac{V_{REF}}{2}\omega$$

$$\Delta T < \frac{\Delta V_{MAX}}{\left.\frac{\partial V_{IN}}{\partial t}\right|_{MAX}} = \frac{V_{REF}/2^{n+1}}{\omega V_{REF}/2}$$

$$\Delta T < \frac{1}{\omega 2^n}$$

Aperture Uncertainty



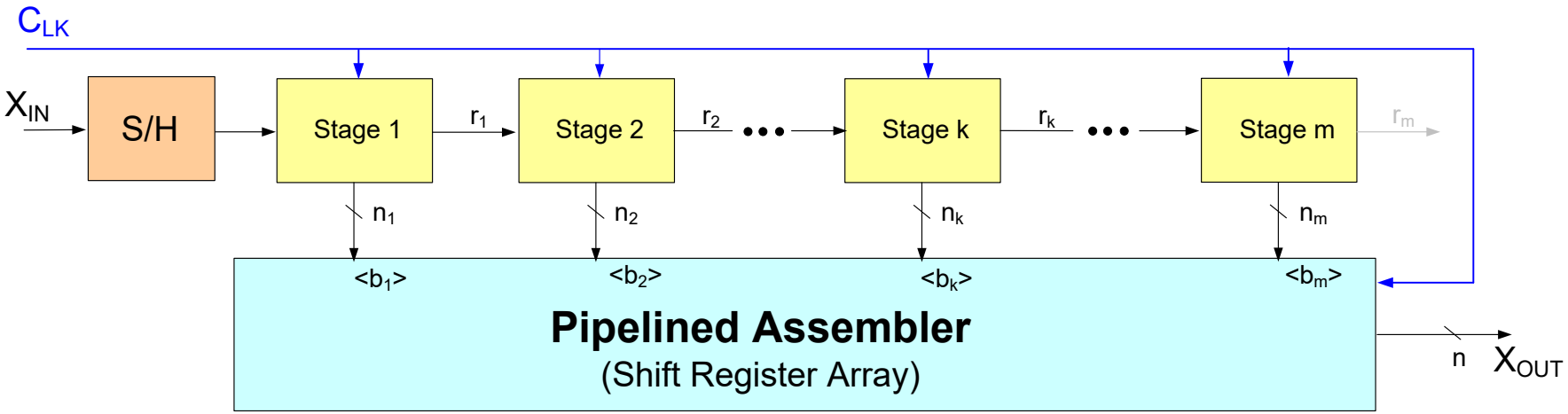
$$\Delta T < \frac{1}{\omega 2^n}$$

Example: If f_{CLK}=200MHz, n=14 determine the aperture uncertainty

$$\Delta T < \frac{1}{2\pi(2E8)2^{14}} = 4.86E\text{-}14 \cong .05\text{p sec}$$

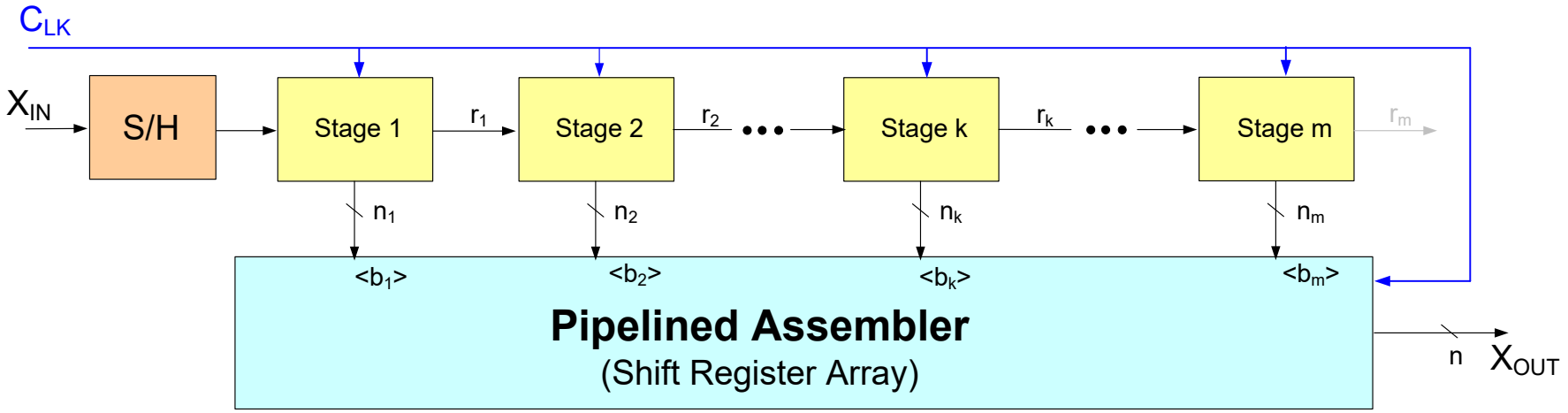
Aperture uncertainty requirements can be very stringent !

Elimination of Input S/H



Why is input S/H used?

Elimination of Input S/H



Why is input S/H used?

Conventional Wisdom:

Because want right output of the first-stage ADC (which is/provides the MSB)
Because gain stages mess up when input is time varying

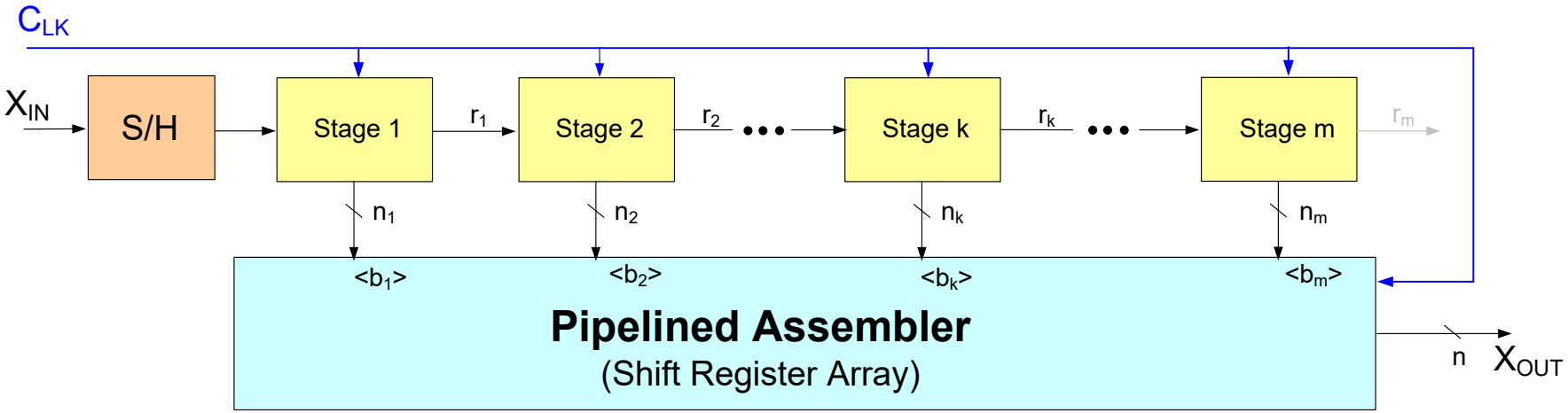
But what does an ADC error do to the Boolean output?

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

Absolutely nothing if over-range protection is provided !

But do need correct value of V_{IN} when creating the residues !!

Elimination of Input S/H



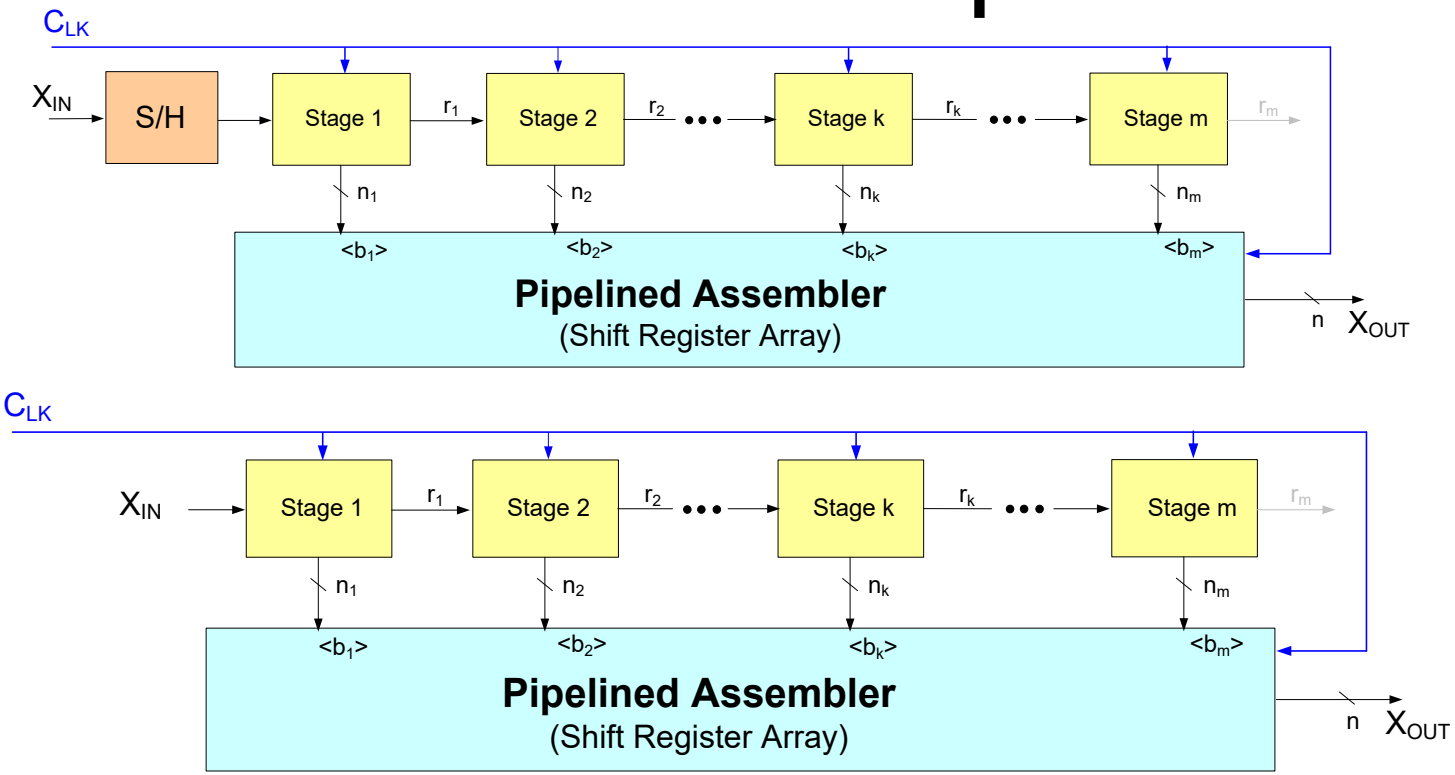
Why is input S/H used?

Conventional Wisdom:

Because want right output of the first-stage ADC (which is/provides the MSB)
Because gain stages mess up when input is time varying

Observation: If SC structures used for the gain stages, there is an inherent sampling that takes place at the input of each stage – including the first stage

Elimination of Input S/H



Advance sampling clock a little so that sample is taken at quiet time but not too much to loose over-range protection

- This simply skews the sampling times
- Probably need to bootstrap the input sampling switch
- Bottom plate sampling

Fully Differential Architectues

Second-order spectral component is often most significant contributor to SFDR and THD limitations in single-ended structures

Noise from ADC and other components, coupled through the substrate, often source of considerable noise in an ADC

- All even-ordered spectral components are eliminated with fully-differential symmetric structures
- Common mode noise is rejected with fully-differential symmetric structures

Almost all implementations of Pipelined ADCs are fully-differential

Straightforward modification of the single-ended concepts discussed here

Authors often present structures in single-ended mode and then just mention that differential structure was used

Modest (but small) increase in area and power for fully differential structures

Signal level increases by factor of 2 and device noise typically increases by $\sqrt{2}$ as well

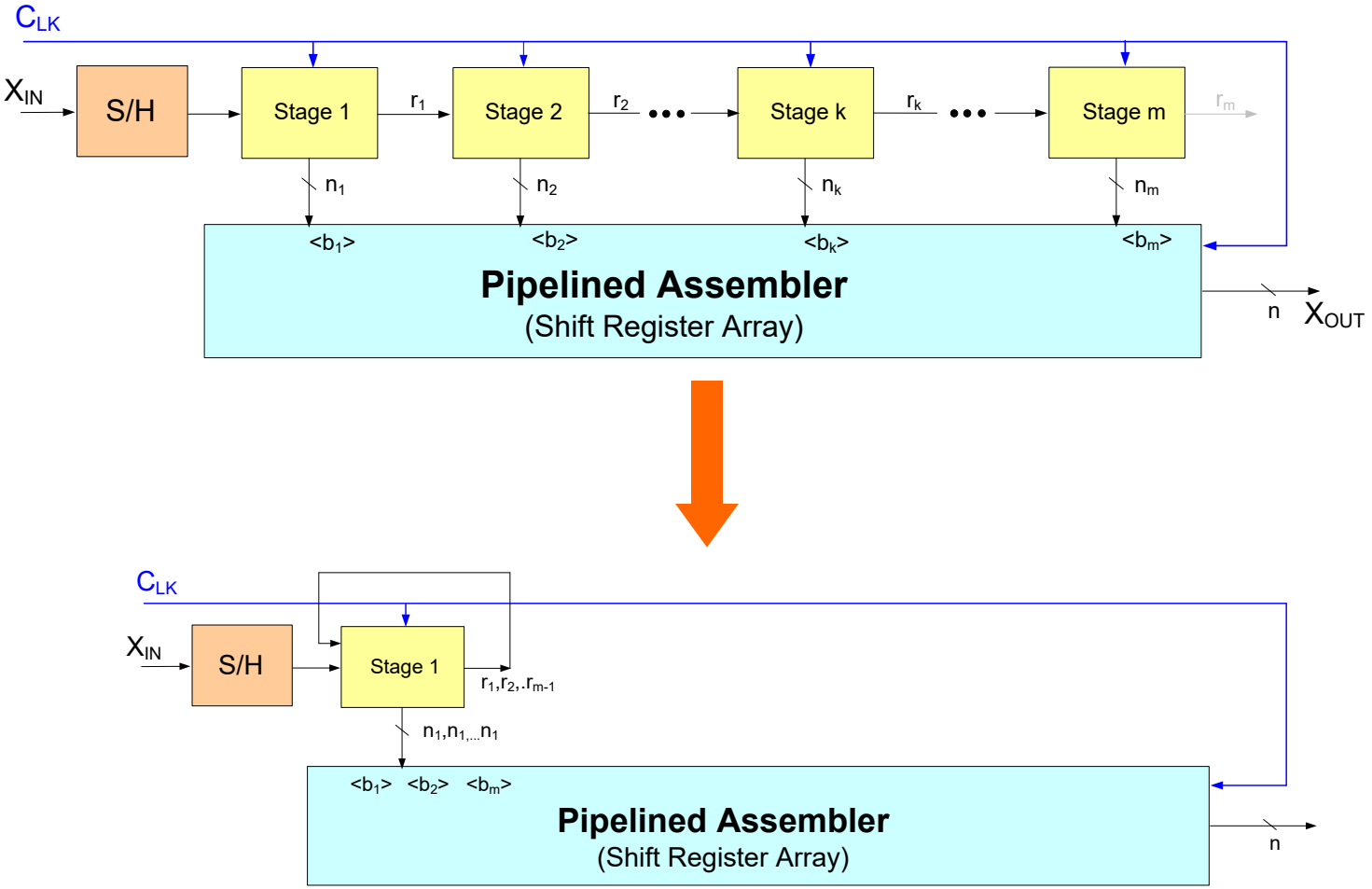
Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Op Amp Gain causes finite gain errors and introduces noninearity	2. a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3. Op amp settling must can cause errors	3. Select GB to meet settling requirements (degrade modestly to account for slewing)
4. Power dissipation strongly dependent upon GB of Op Amps	4. Minimize C_L, use energy efficient op amps, share or shut down op amp when not used,scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies. Good (near optimal) noise distribution strategy should be followed.
5. Choice of FB Amplifier Architecture seriously impacts performance	5. Bottom plate sampling, bootatrapping, clock advance to reduce aperature uncertainty,critical GB, parasitic insensitivity needed, β dependent upon architecture and phase, compensation for worst-case β, TG if needed
6. Correct interpretation of α_k's is critical	6. a) Accurately set α_k values b) Use analog or digital calibration

Pipelined Data Converter Design Guidelines

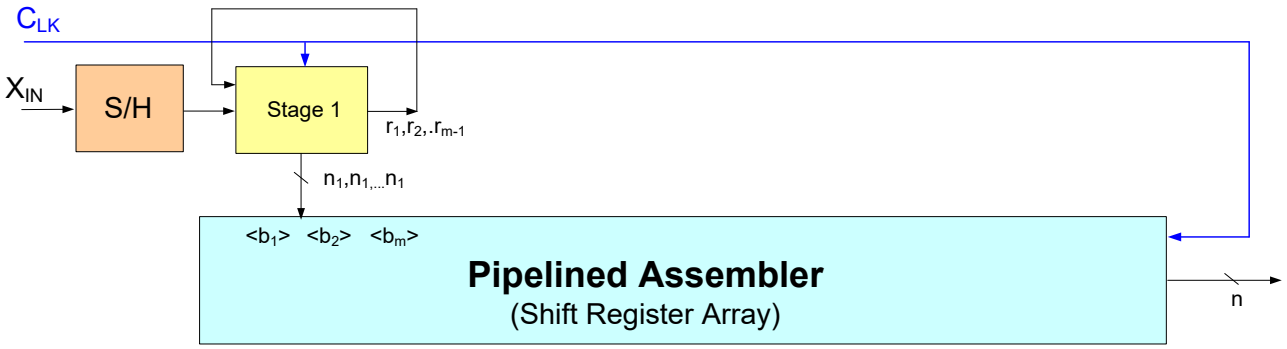
	Issue	Strategy
7.	Sampling operation inherently introduces a sampled-noise due to noise in resistors	Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage) .
8.	Signal-dependent tracking errors at input introduce linearity degradation	Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches
9.	Aperature uncertainty can cause serious errors	Since latency usually of little concern, be sure that a clean clock is used to control all sampling.
10.	Input S/H major contributor to nonlinearity and power dissipation	Eliminate S/H but provide adequate over-range protection for this removal. Reduces power dissipation and improves linearity!
11.	Data converters often have stringent SNR and SNDR requirements	Use fully differential structures to obtain dramatic improvements in SNR and SNDR

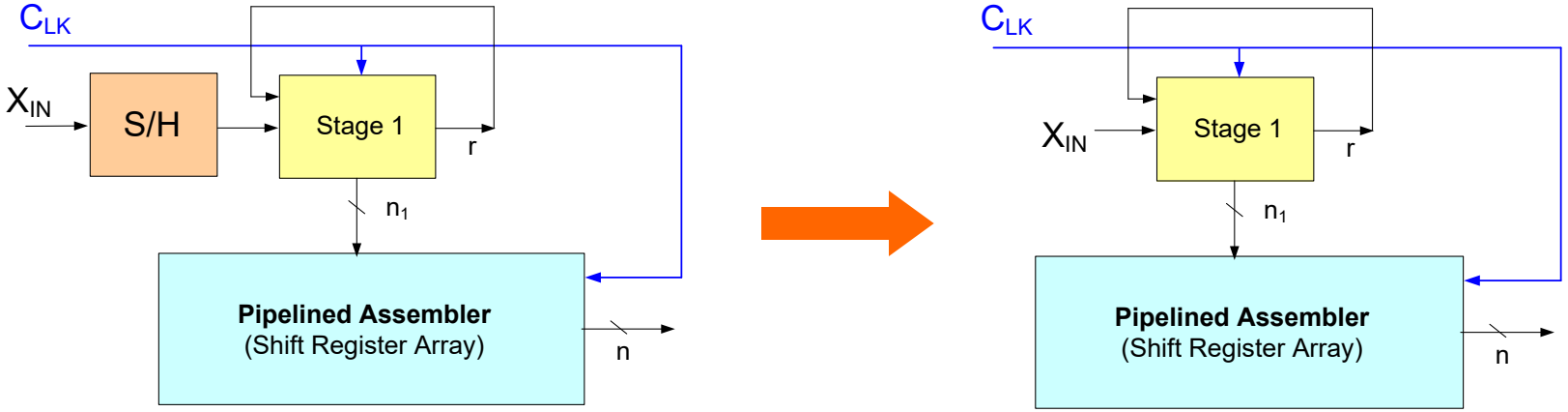
Cyclic (Algorithmic) ADCs



Cyclic (algorithmic) ADC
Reduces throughput but also area

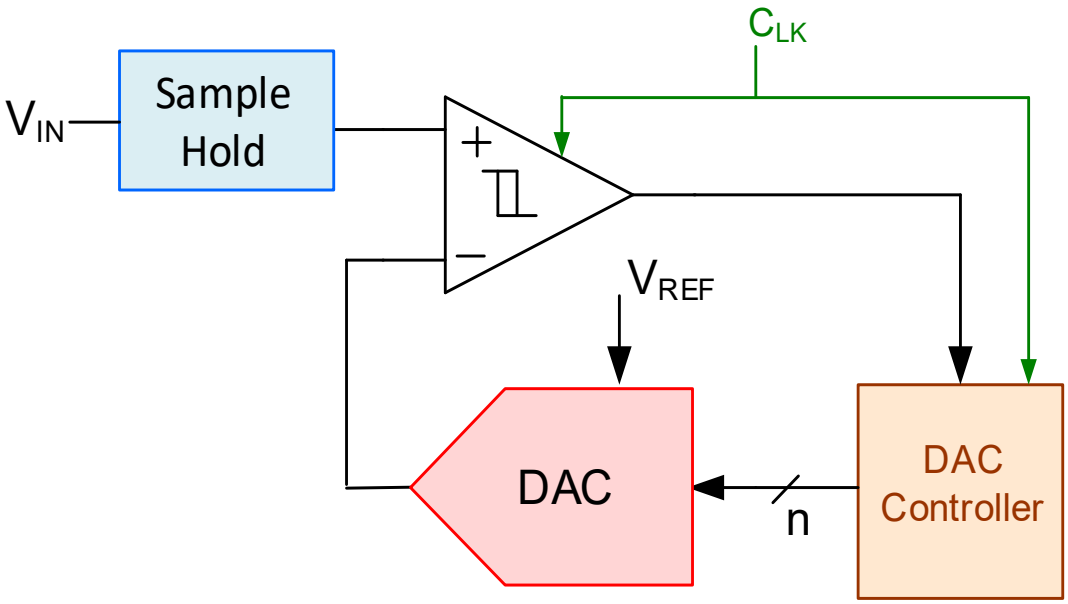
Cyclic (Algorithmic) ADCs





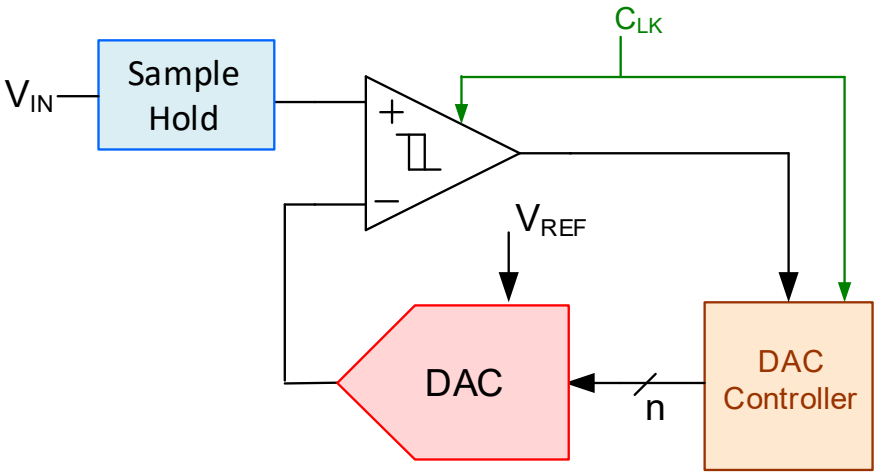
Can bypass bootstrap after initial sample is taken

SAR ADC



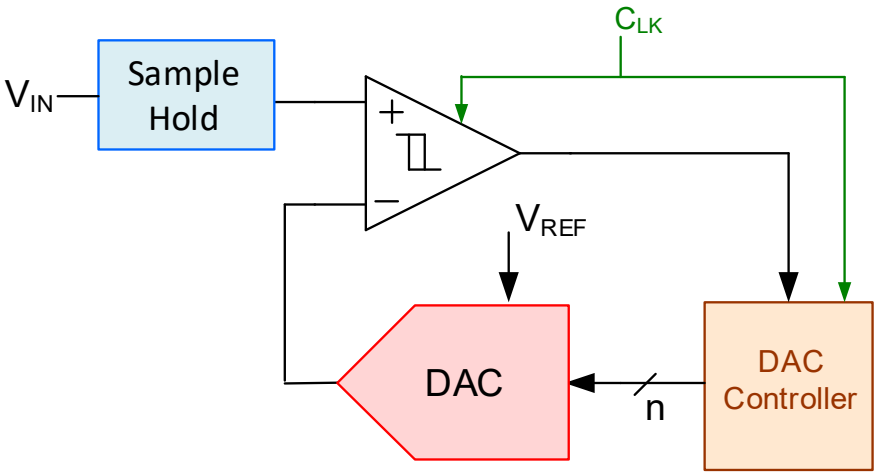
- DAC Controller stores estimates of input in Successive Approximation Register (SAR)
- At end of successive approximation process, ADC output is in SAR
- Eliminates the power-consuming amplifiers of the pipelined ADC
- Much slower than pipelined ADC
- S/H at the input is essential
- Can have excellent power performance
- Widely used structure with renewed attention in recent years

SAR ADC



- Any DAC structure can be used
- In basic structure, single comparator can be used
- Performance entirely determined by S/H, DAC, and comparator
- Very simple structure and relatively fast design procedure
- If offset voltage of comparator is fixed, comparator offset will not introduce any nonlinearity

SAR ADC



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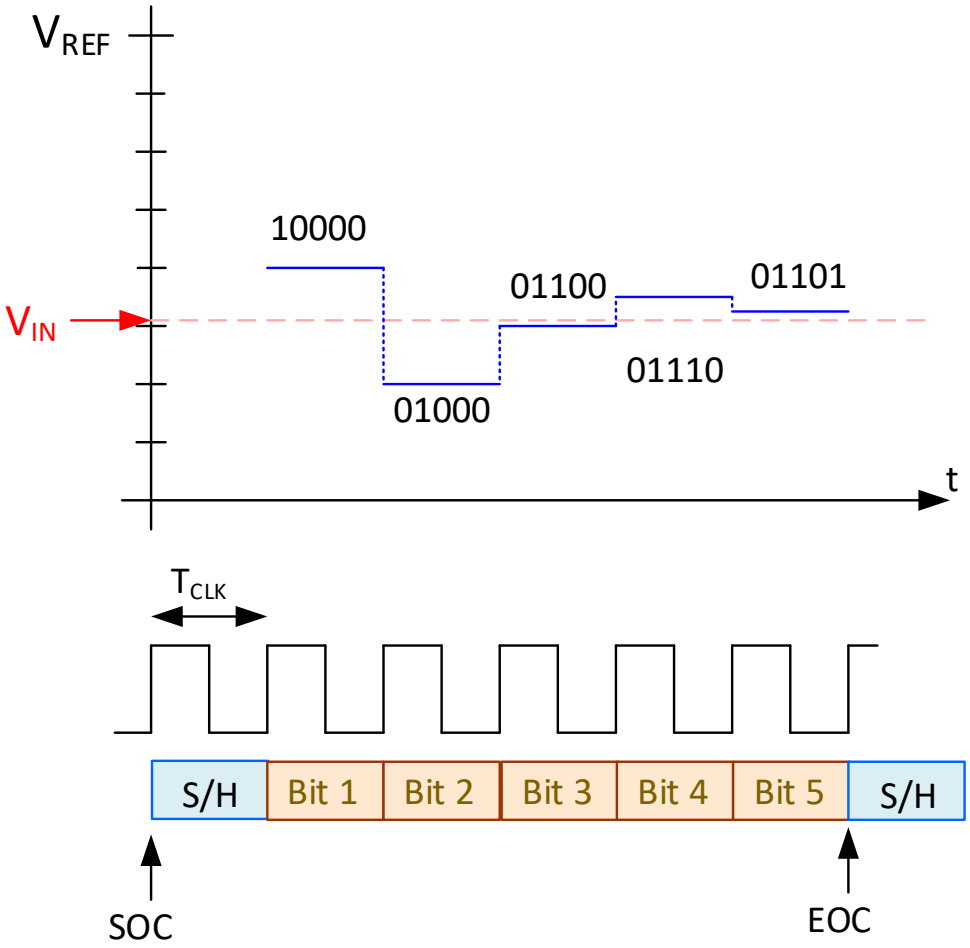
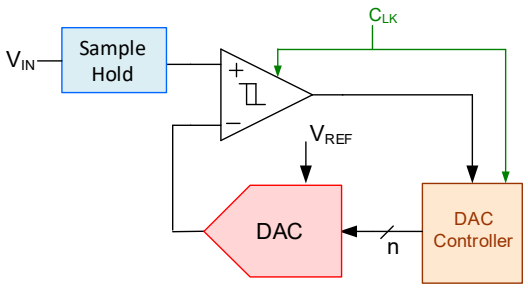
SAR ADC

Typical Operation (shown for 5 bits)

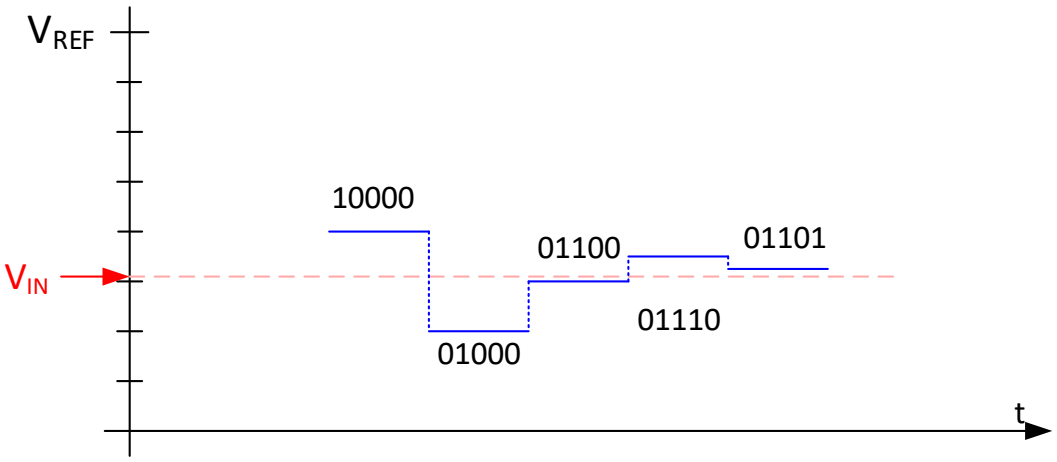


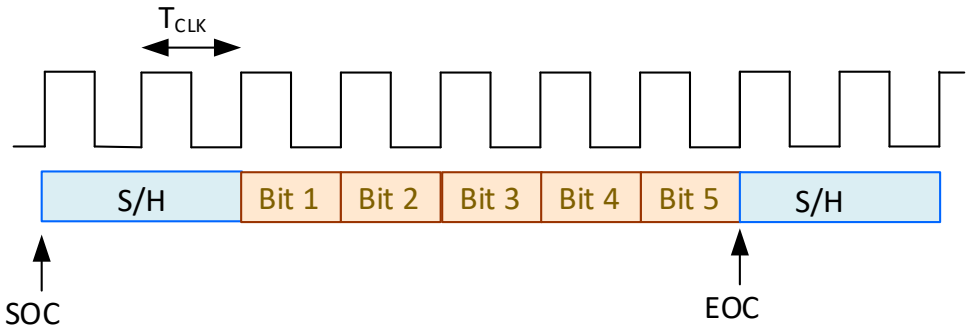


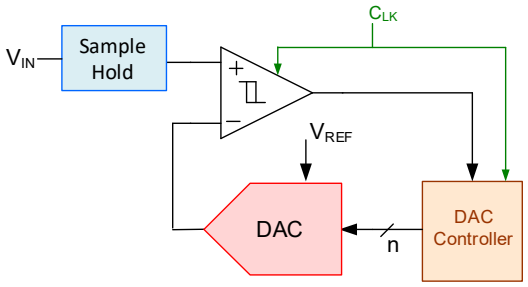
- Requires n+1 clock cycles
- Can be extended to large number of bits (16 or more)
- Comparator requires large CM range
- Previous-code dependence of comparator offset voltage must be managed
- Speed limited by S/H

SAR ADC

Typical Operation (shown for 5 bits)

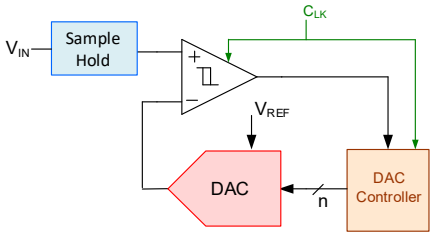




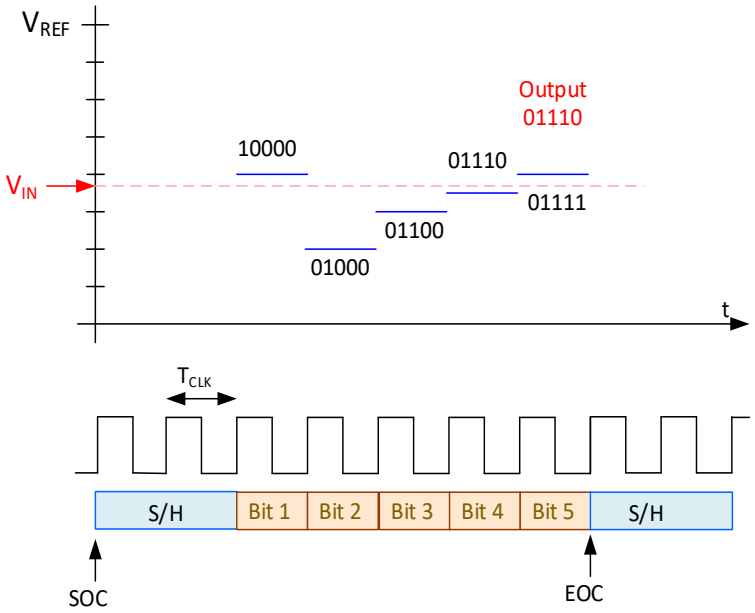


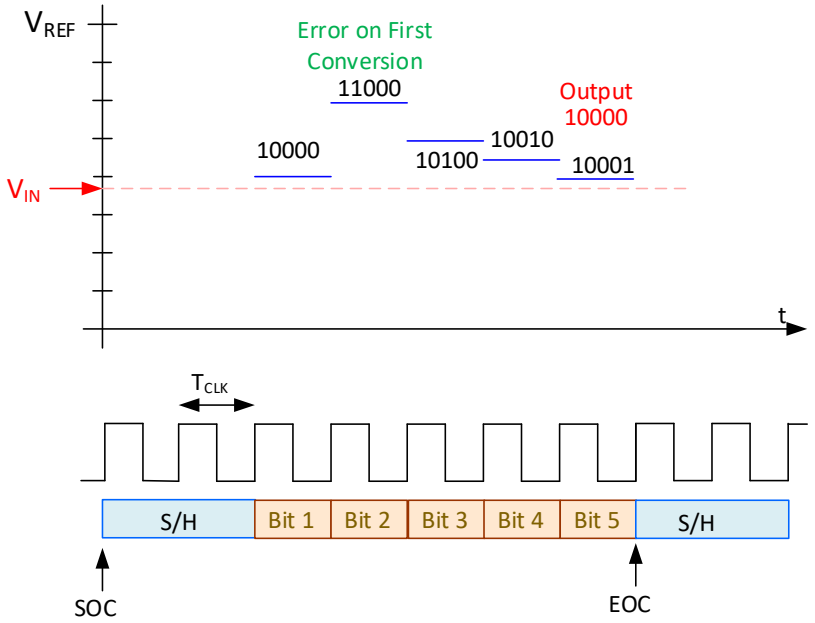
- Two or more bit periods can be added to S/H
- Slows overall operation proportionally but overhead small for large n

SAR ADC



- Does not recover from errors
- Particularly problematic when errors occur on earlier bits
- Over-range protection can be added but at expense of additional clock periods





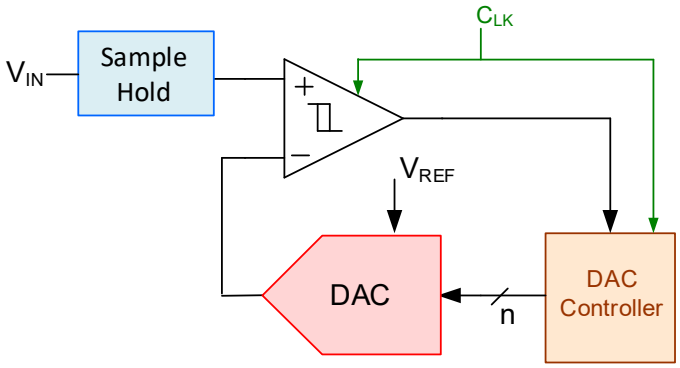
SAR ADC

Note notation difference

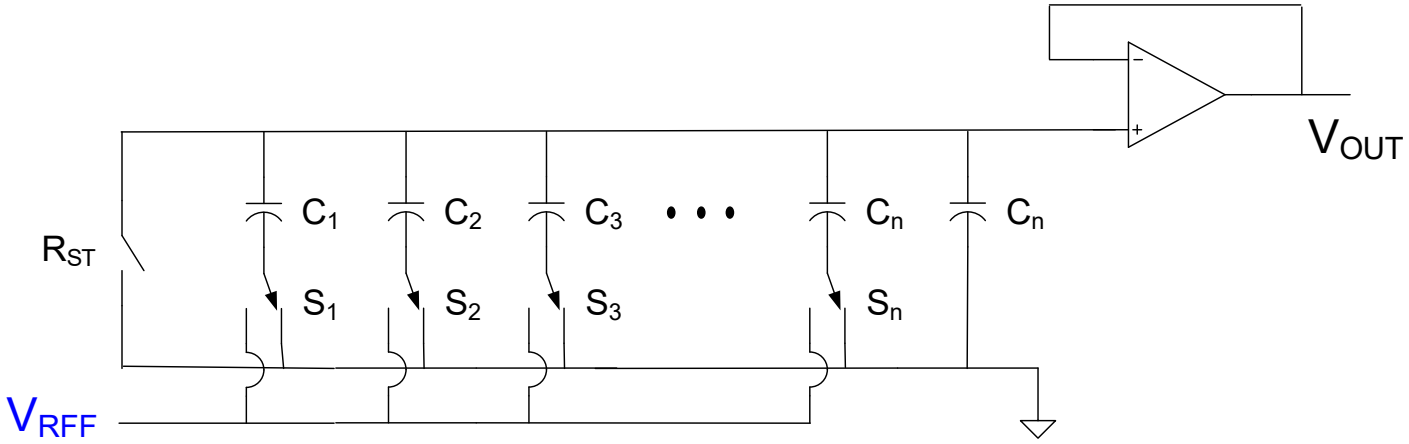
$\vec{X}_{OUT}=<d_{n-1},d_{n-2},\ldots d_0>$

d_0 is the Least Significant Bit (LSB)

d_{n-1} is the Most Significant Bit (MSB)

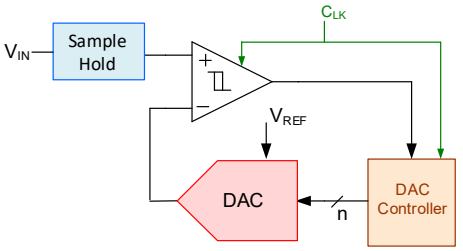


Charge Redistribution DAC could be used in SAR ADCs

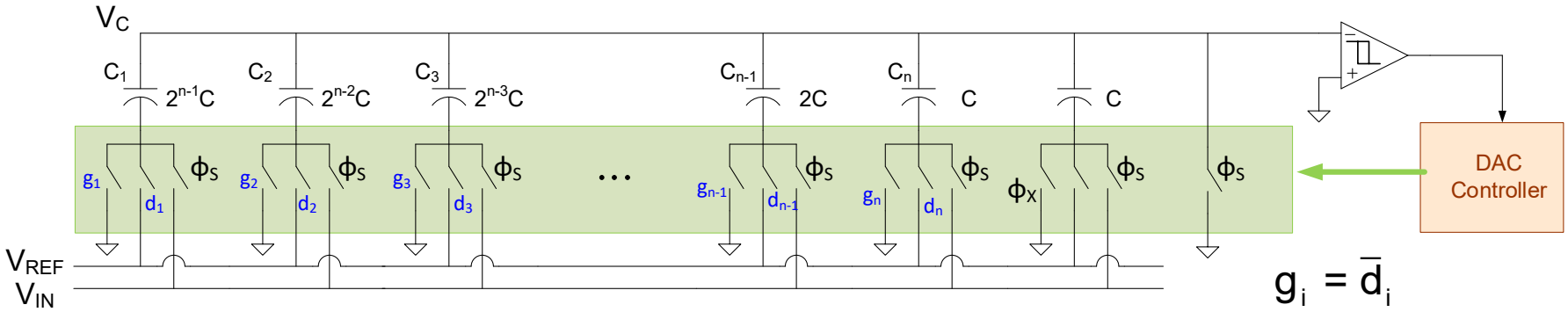


- Capacitors usually binary weighted
- With this DAC, typical common-mode input required for comparator
- Standard S/H also required

SAR ADC

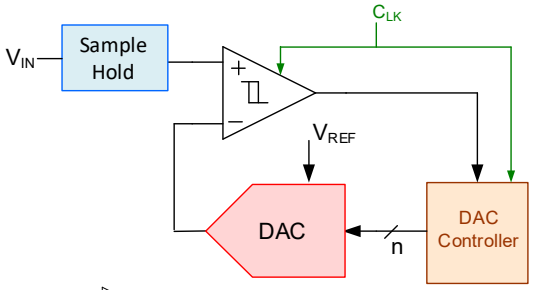


Alternate Charge Redistribution DAC

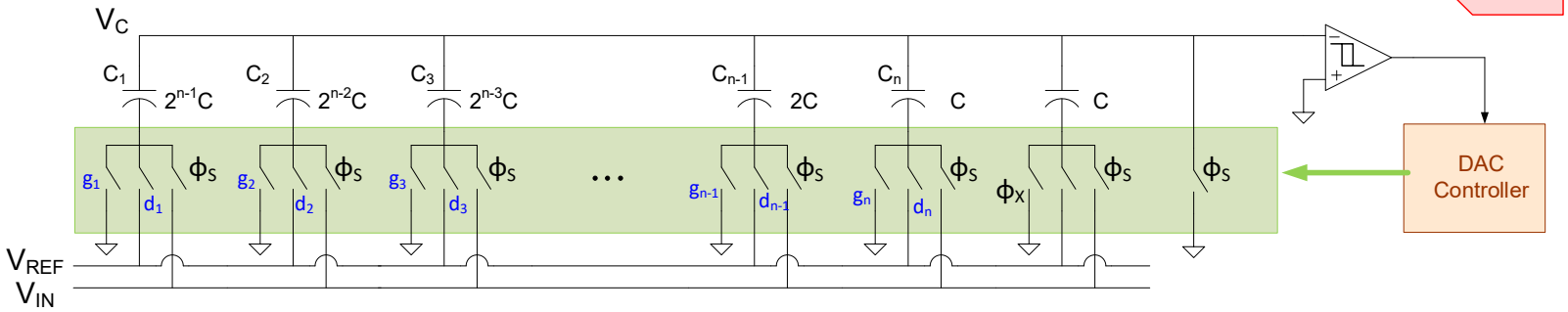


- During sampling phase, input is sampled on all capacitors
- During successive approximation process, capacitors are alternately connected to ground or V_{REF}
- Voltage on common node will converge to 0
- Comparator is always comparing to ground thus reducing common-mode nonlinearity errors
- Previous code dependence of comparator still of concern
- Note input sample is <u>not</u> held independently throughout the entire conversion process
- Bootstrapped switch is critical during sampling phase
- Parasitic capacitances on V_C node do not affect final output (Bottom plate)
- Major source of power dissipation is in the charge redistribution process

SAR ADC



Alternate Charge Redistribution DAC



$$C_i = C2^{n-i} \qquad 1 \le i \le n$$

Define Q to be the charge sampled onto capacitors

$Q = Q_{SAMP}$ and define $g_i = \overline{d}_i$ and $\phi_X = \overline{\phi}_S$

$$Q = 2^n CV_{IN}$$

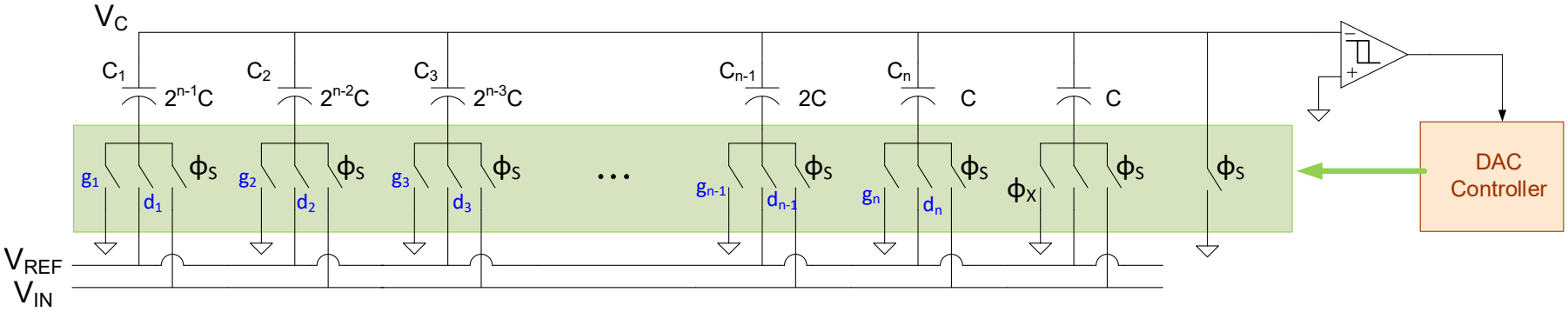
$$Q = \sum_{i=1}^{n} C_i \left(d_i V_{REF} - V_C \right) - CV_C$$

$$Q = \sum_{i=1}^{n} C2^{n-i} \left(d_i V_{REF} - V_C \right) - CV_C = CV_{REF} \sum_{i=1}^{n} d_i 2^{n-i} - CV_C \left(\sum_{i=1}^{n} 2^{n-i} + 1 \right)$$

$$\Rightarrow \quad Q = CV_{REF} \sum_{i=1}^{n} d_i 2^{n-i} - CV_C \left(2^n \right)$$

SAR ADC

Alternate Charge Redistribution DAC



$$CV_{REF}\sum_{i=1}^{n} d_i 2^{n-i} - CV_C\left(2^n\right) = 2^n CV_{IN}$$

$$V_{IN} = V_{REF}\sum_{i=1}^{n} d_i \frac{2^{n-i}}{2^n} - V_C$$

$$V_{IN} = V_{REF}\sum_{i=1}^{n} d_i 2^{-i} - V_C$$

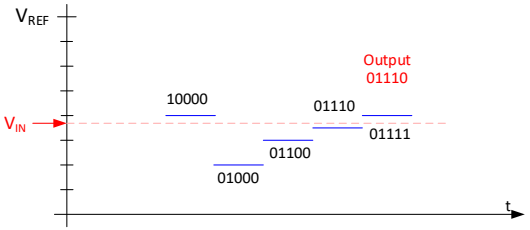
If the SAR output is adjusted so that

$$-\frac{V_{REF}}{2^n} \le V_C \le \frac{V_{REF}}{2^n}$$

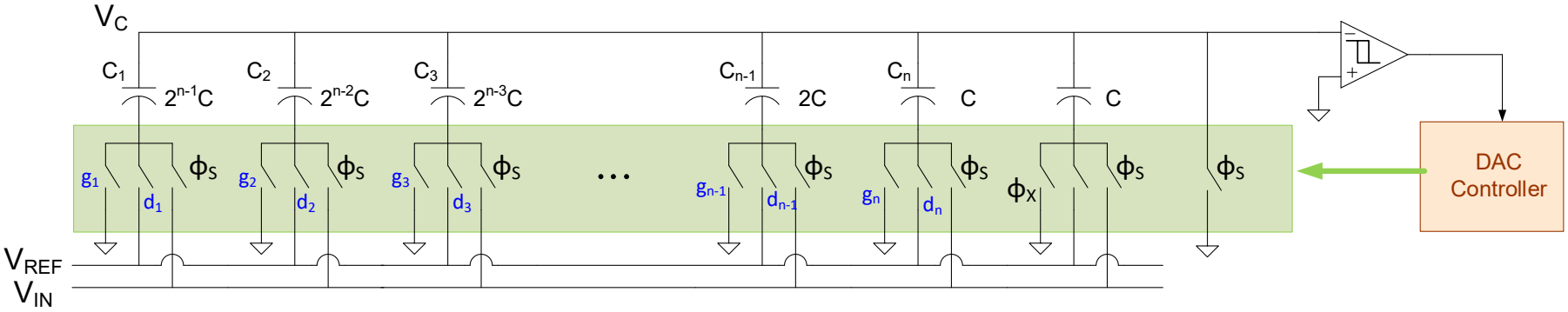
It follows that

$$V_{REF}\sum_{i=1}^{n} d_i 2^{-i} - \frac{V_{REF}}{2^n} \le V_{IN} \le V_{REF}\sum_{i=1}^{n} d_i 2^{-i} + \frac{V_{REF}}{2^n}$$

SAR ADC



Alternate Charge Redistribution DAC



Binary Search Process Description

1. After sampling V_{IN} with φ_S, envision closing all g switches and φ_X V_C will be $-V_{IN}$.
2. Close d_1 (i.e. guess d_1=1) It follows that

$$C_1(V_{REF} - V_C) - \sum_{i=2}^{n} C_i V_C - CV_C = \sum_{i=1}^{n} C_i V_{VIN} + CV_{IN}$$

solving obtain $V_C = 2^{-1}V_{REF} - V_{IN}$

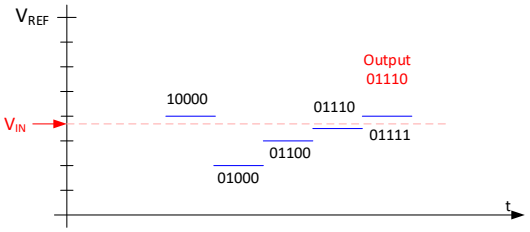
thus $V_C > 0 \Rightarrow d_1 = 0$

3. Since d_1=0, close g_1 and now close d_2 (i.e. guess d_2=1). It follows that

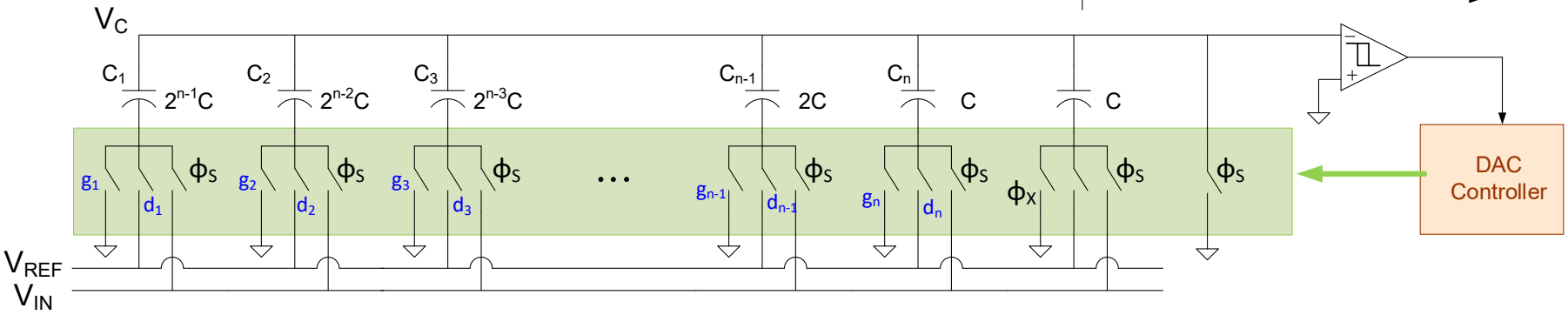
$$V_C = 2^{-2}V_{REF} - V_{IN}$$

thus $V_C < 0 \Rightarrow d_2 = 1$

SAR ADC



Alternate Charge Redistribution DAC



Binary Search Process Description

4. Since d_2=1, leave d_2 closed and now close d_3 (i.e. guess d_3=1). It follows that

$$V_C = 2^{-3}V_{REF} + 2^{-2}V_{REF} - V_{IN}$$

thus $V_C > 0 \Rightarrow d_3 = 0$

5. Since d_3=0, open d_3 and now close d_4 (i.e. guess d_4=1). It follows that

$$V_C = 2^{-4}V_{REF} + 2^{-2}V_{REF} - V_{IN}$$

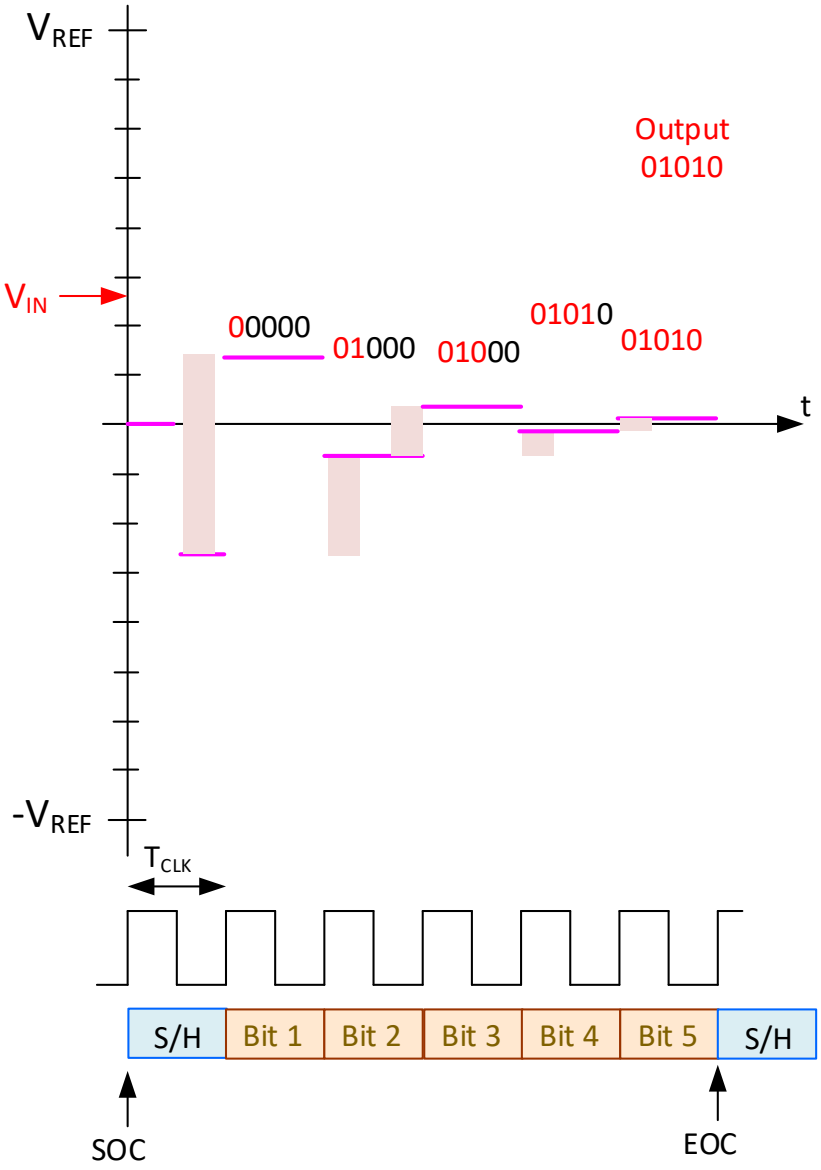
thus $V_C < 0 \Rightarrow d_4 = 1$

6. Since d_4=1, keep d_4 closed and now close d_5 (i.e. guess d_5=1) . It follows that

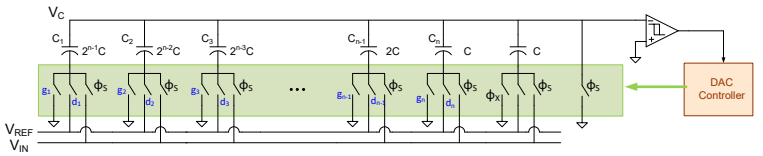
$$V_C = 2^{-5}V_{REF} + 2^{-4}V_{REF} + 2^{-2}V_{REF} - V_{IN}$$

thus $V_C > 0 \Rightarrow d_5 = 0$

SAR ADC

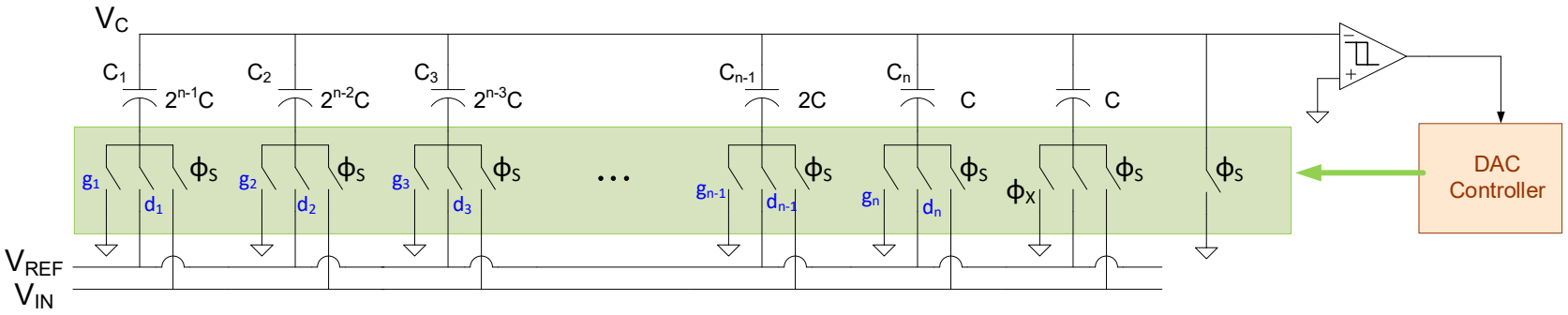


Alternate Charge Redistribution DAC



SAR ADC

C-2C Array for Charge Redistribution DAC



Can a C-2C array be used for the charge-redistribution DAC?

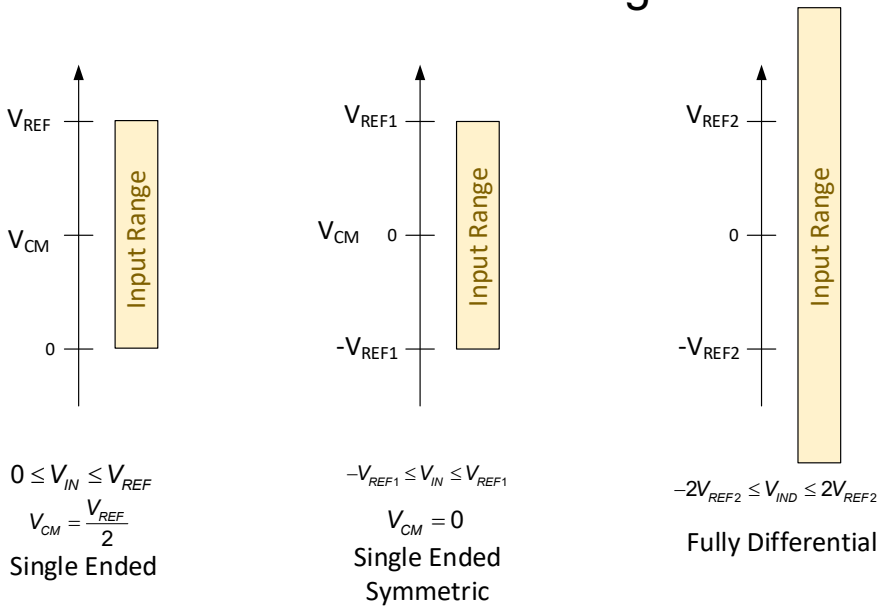
Yes – but internal nodes would all need to settle !

Can a counter be used rather than a binary search to obtain the SAR code?

Yes – but conversion time would be long with worst-case requiring 2^n periods

SAR ADC

- Concepts are often expressed in single-ended structures
- Fully differential structures widely used
- Distinction between reference voltages often not clearly stated



Is Common-Mode input 0 or $V_{REF}/2$?
Is maximum input V_{REF}, $2V_{REF}$ or $4V_{REF}$:

- Single-ended V_{REF}
- Single-ended Differential Input $+V_{REF}$, $-V_{REF}$
- Differential Input

Example of Fully Differential Implementation

United States Patent [19]
Hester et al.

[11] **Patent Number:** 4,803,462
[45] **Date of Patent:** Feb. 7, 1989

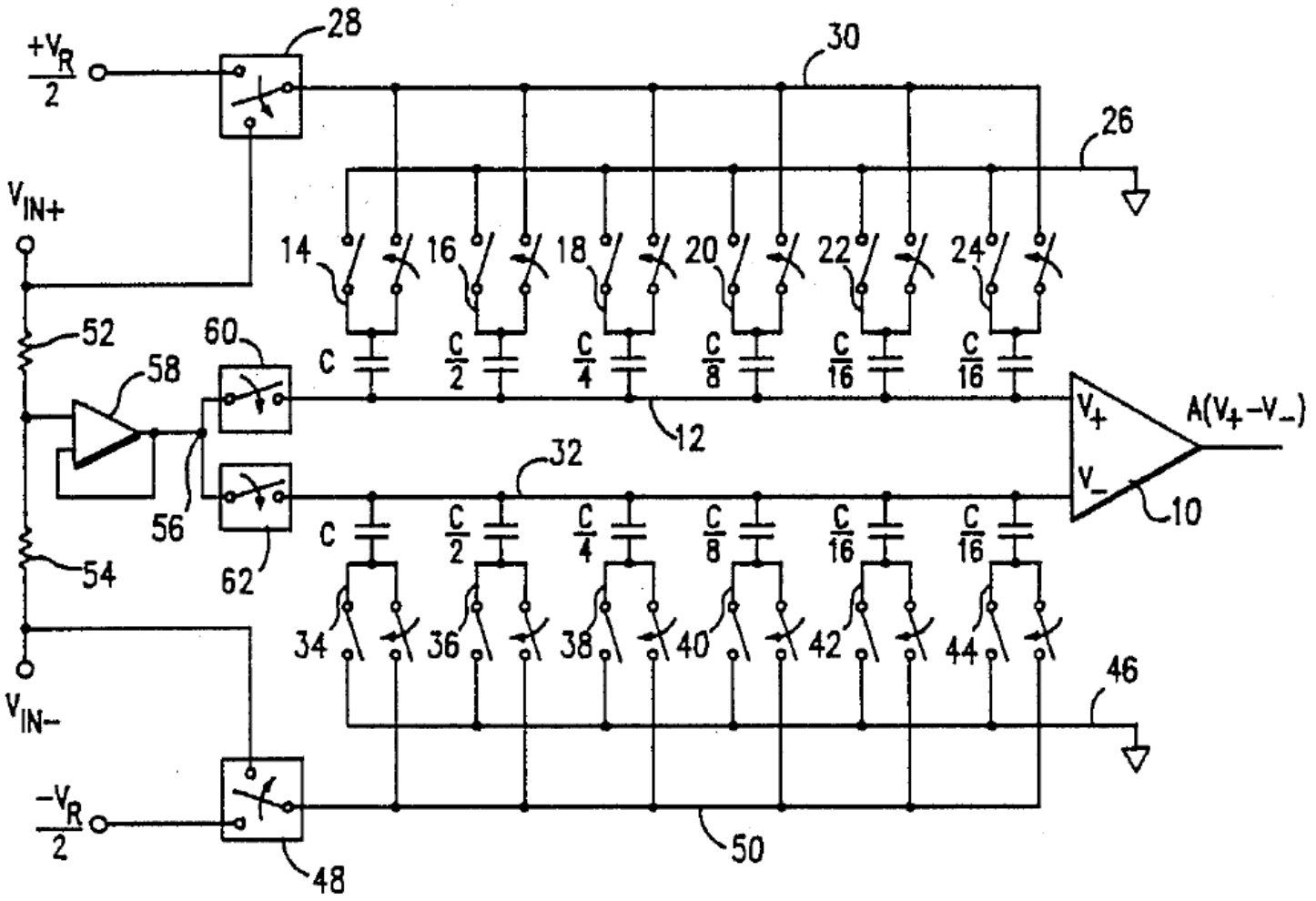
[54] **CHARGE REDISTRIBUTION A/D CONVERTER WITH INCREASED COMMON MODE REJECTION**

[75] Inventors: **Richard K. Hester**, Whitewright; **Michiel de Wit**, Dallas, both of Tex.

Primary Examiner—T. J. Sloyan
Attorney, Agent, or Firm—Stanton C. Braden; James T. Comfort; Melvin Sharp

[57] **ABSTRACT**

An A/D converter includes a positive array of binary



Another example of Fully Differential Implementation with different switching sequence and different references.

United States Patent [19] [11] **Patent Number:** **4,803,462**
Hester et al. [45] **Date of Patent:** **Feb. 7, 1989**

[54] **CHARGE REDISTRIBUTION A/D CONVERTER WITH INCREASED COMMON MODE REJECTION**

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[57] **ABSTRACT**

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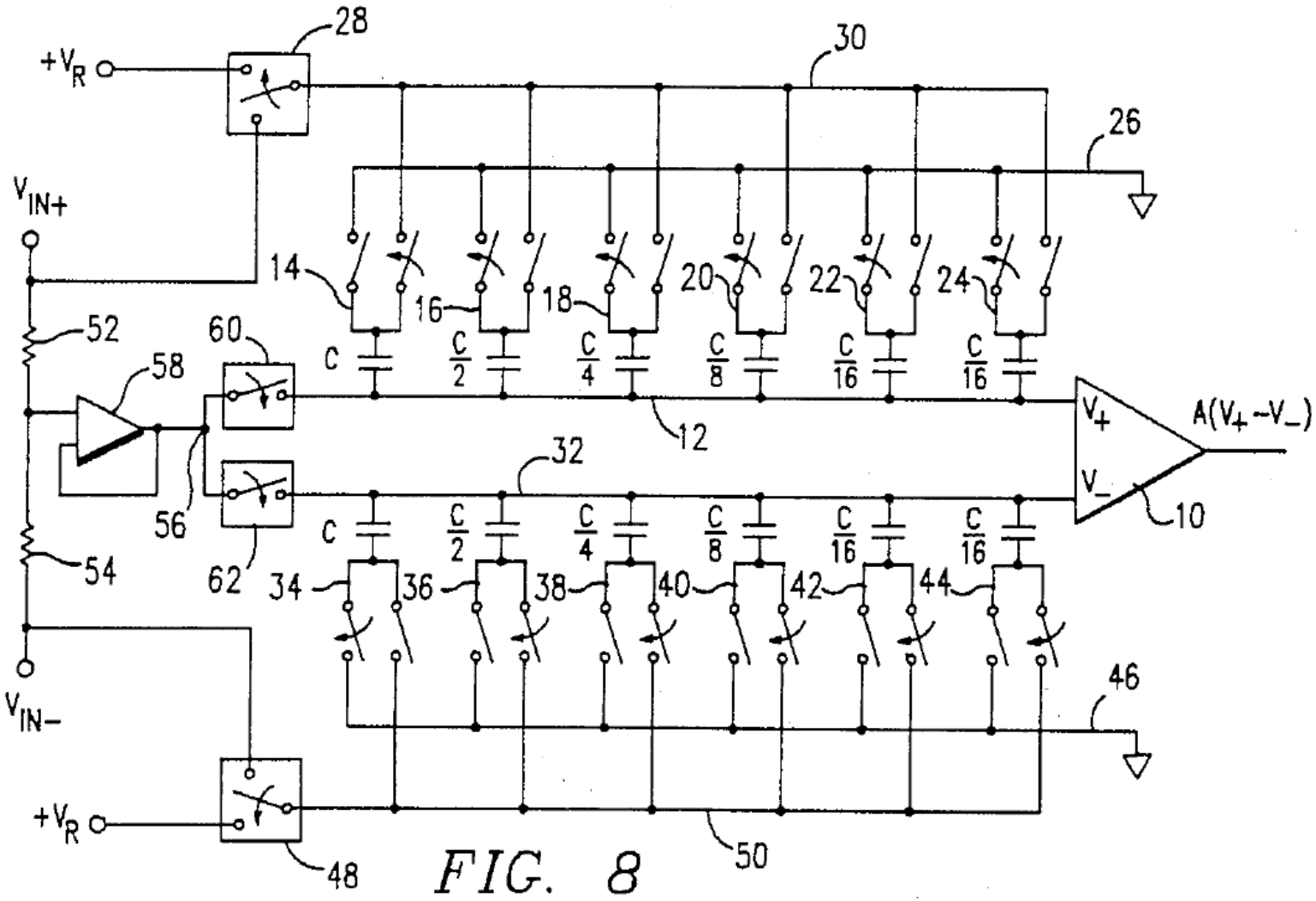


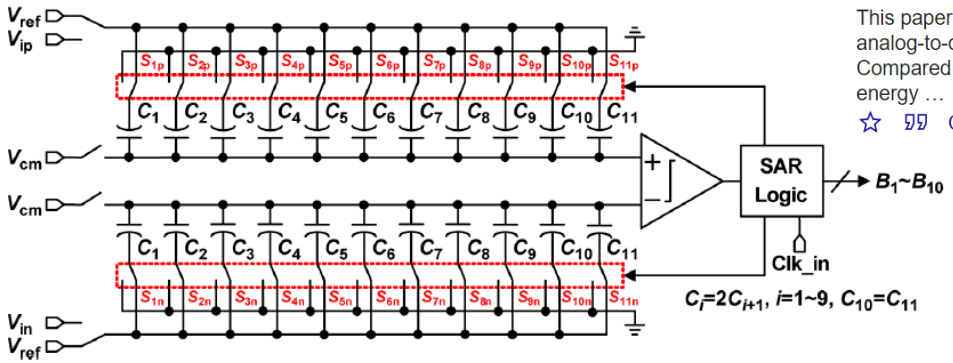
FIG. 8

SAR ADC

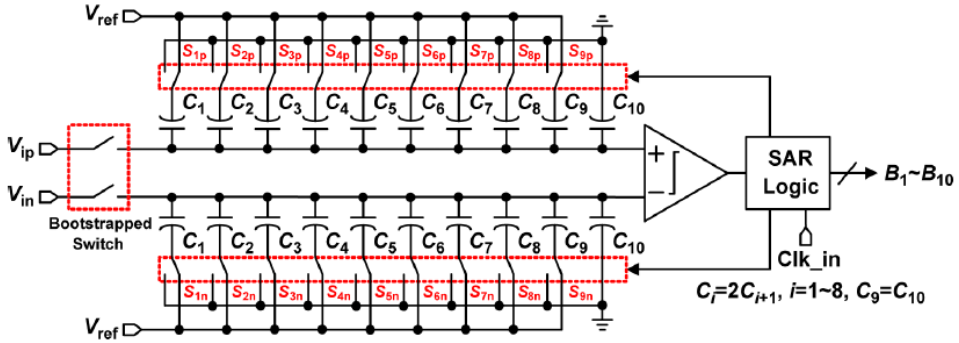
Charge Redistribution ADC with reduced charge redistribution energy

Goal: Reduce unnecessary switching inherent in the original process by first switching all capacitors to V_{REF} and then returning to ground if test fails.

Goal: Only switch if needed!



Standard Switching



Reduced Switching

[PDF] **A 10-bit** 50-MS/s **SAR ADC** with **a monotonic capacitor** switching procedure

CC Liu, SJ Chang, GY Huang… - IEEE Journal of Solid …, 2010 - msicdt.ee.ncku.edu.tw

This paper presents **a** low-power **10-bit** 50-MS/s suc-cessive approximation register (**SAR**) analog-to-digital converter (**ADC**) that uses **a monotonic capacitor** switching procedure. Compared to converters that use **the** conventional procedure, **the** average switching energy …

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[PDF] ncku.edu.tw

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550 (April 2017 I believe)
788 (4/17/2019)

Samples input on array connected between V_{IN} and V_{REF}

Only change state if output must be decreased

For 10-bit ADC, reported switching energy and total capacitance reduced by about 81% and 50%, respectively

Does not consider kT/C noise since resolution is small

SAR ADC

Charge Redistribution ADC with reduced charge redistribution energy

Goal: Only switch if needed!

[PDF] **A 10-bit** 50-MS/s **SAR ADC** with **a monotonic capacitor** switching procedure
CC Liu, SJ Chang, GY Huang… - IEEE Journal of Solid …, 2010 - msicdt.ee.ncku.edu.tw
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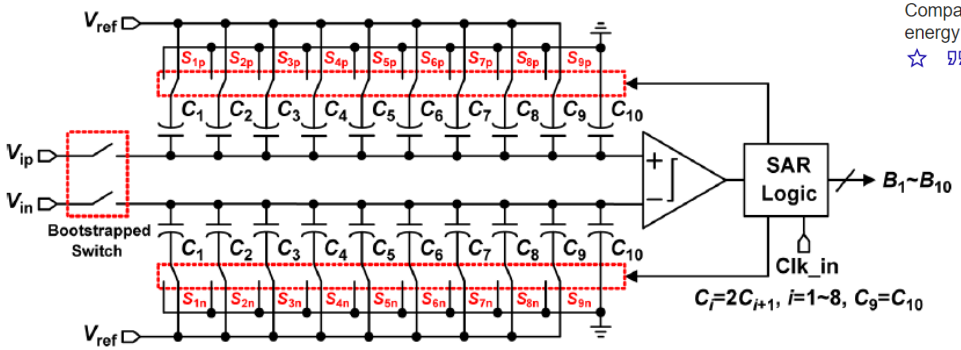
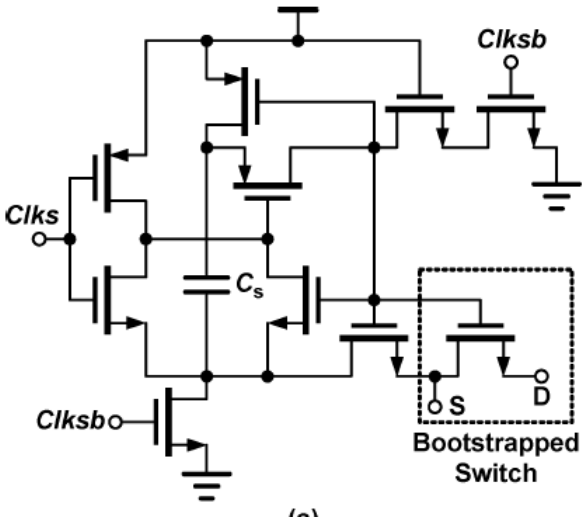
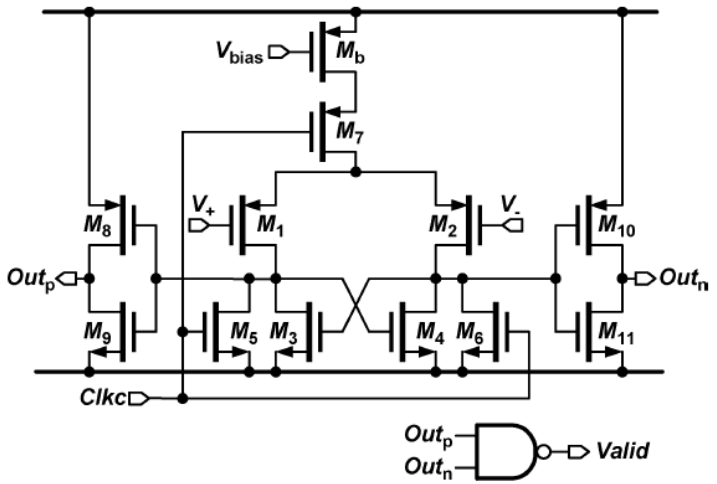
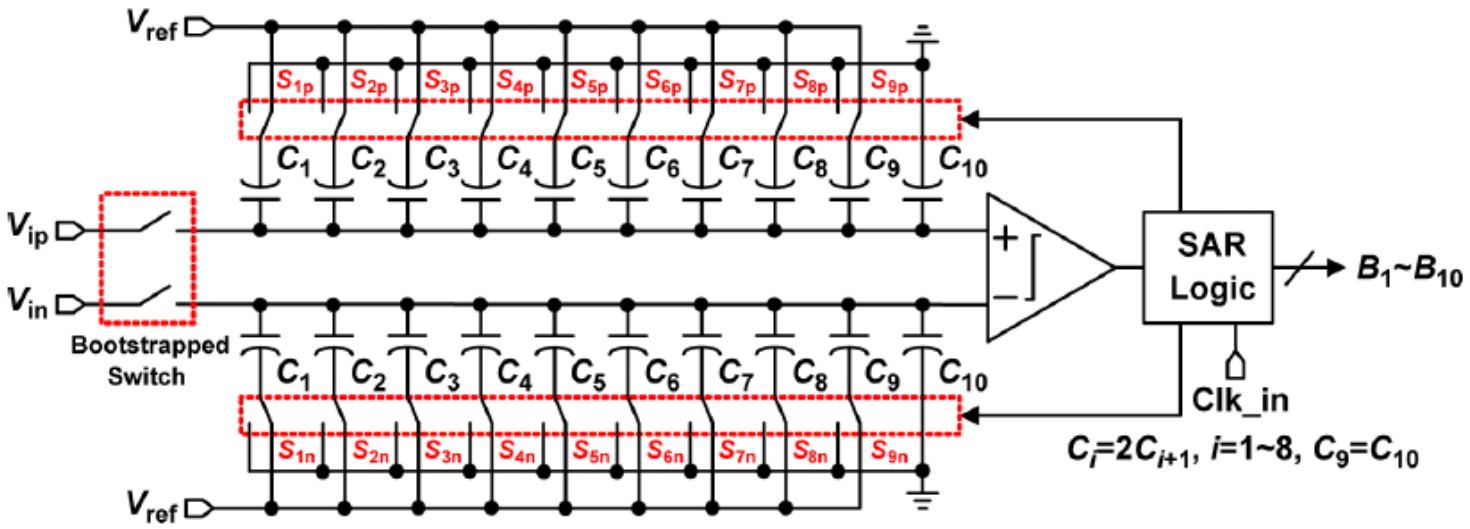
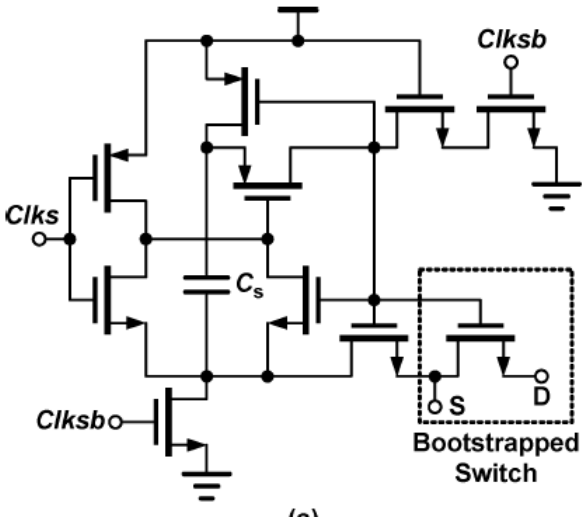


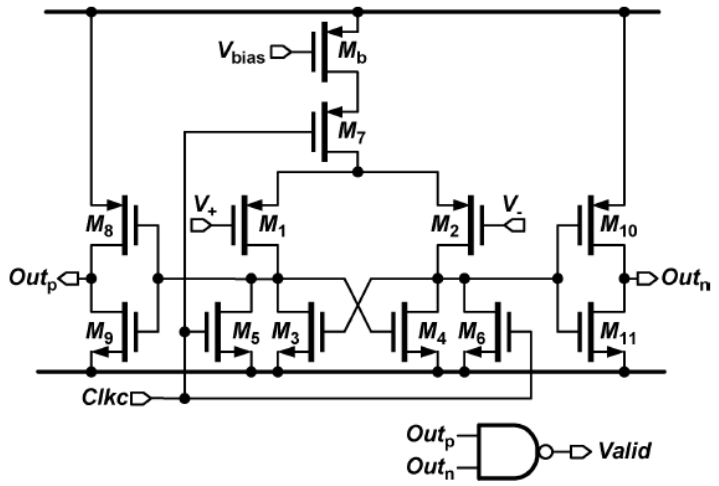




SAR ADC


V_{ref}
S_{1p} S_{2p} S_{3p} S_{4p} S_{5p} S_{6p} S_{7p} S_{8p} S_{9p}
C_1 C_2 C_3 C_4 C_5 C_6 C_7 C_8 C_9 C_{10}
V_{ip}
V_{in}
Bootstrapped Switch
S_{1n} S_{2n} S_{3n} S_{4n} S_{5n} S_{6n} S_{7n} S_{8n} S_{9n}
V_{ref}
SAR Logic
B_1~B_{10}
Clk_in
$C_i=2C_{i+1}$, i=1~8, $C_9=C_{10}$


Clksb
Clks
C_s
S
D
Clksb
Bootstrapped Switch


V_{bias}
M_b
M_7
V_+
V_-
M_8
M_1
M_2
M_{10}
Out_p
Out_n
M_9
M_5 M_3
M_4 M_6
M_{11}
Clkc
Out_p
Out_n
Valid

SAR ADC

Charge Sharing ADC with reduced charge redistribution energy

Goal: Have only passive switching

[PDF] **A 10-bit** 50-MS/s **SAR ADC** with **a monotonic capacitor** switching procedure
CC Liu, SJ Chang, GY Huang… - IEEE Journal of Solid …, 2010 - msicdt.ee.ncku.edu.tw
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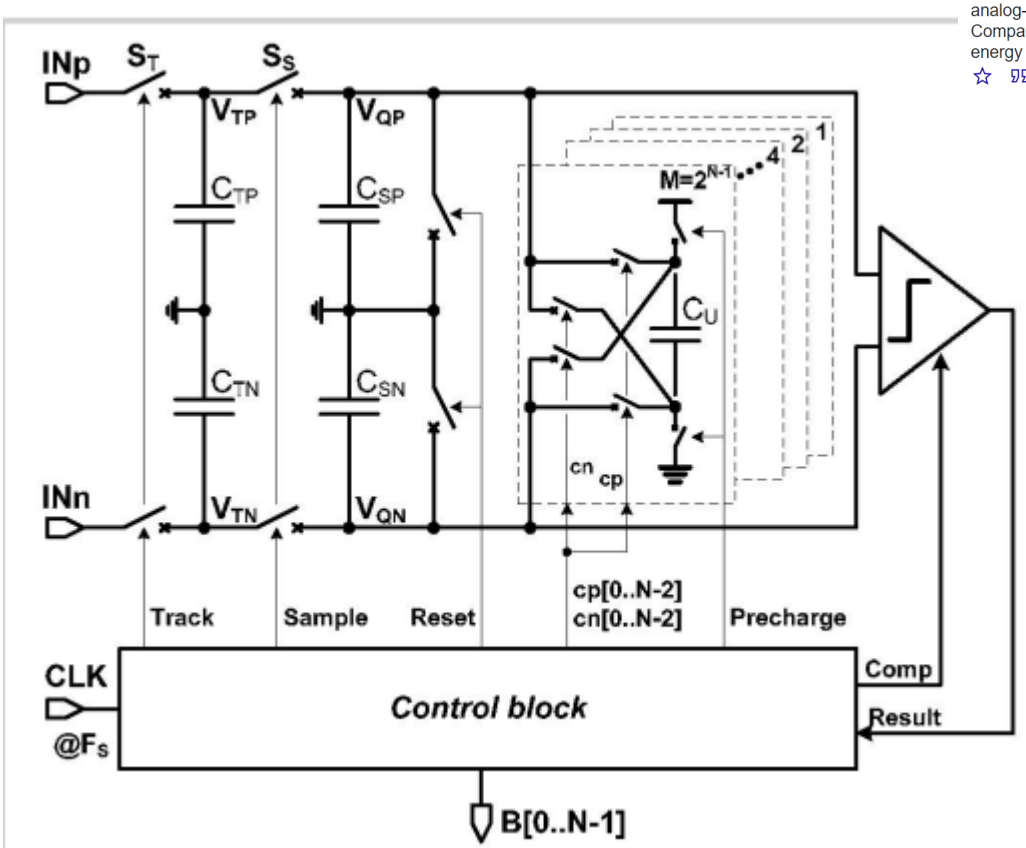
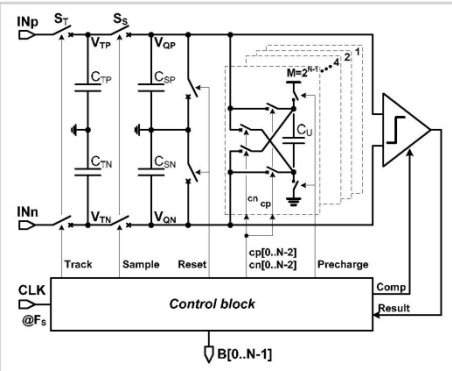


SAR ADC

Charge Sharing ADC with reduced charge redistribution energy

Goal: Have only passive switching



A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7 mW 9b charge-sharing **SAR ADC** in 90nm digital CMOS

J Craninckx, G Van der Plas - Solid-State Circuits Conference, …, 2007 - ieeexplore.ieee.org

Abstract: A fully dynamic **SAR ADC** is proposed that uses passive charge-sharing and an asynchronous controller to achieve low power consumption. No active circuits are needed for high-speed operation and all static power is removed, offering power consumption

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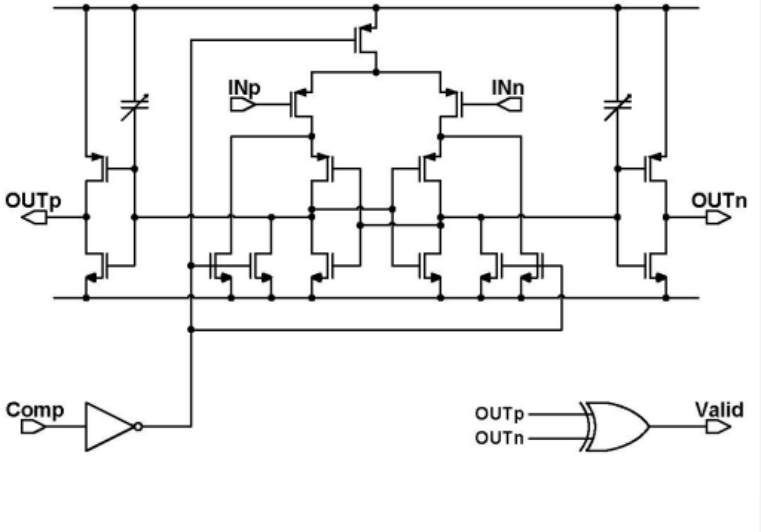

SAR ADC

Lots of ongoing activity in SAR ADCs

A 14-b 20-MS/s 78.8 dB-SNDR energy-efficient **SAR ADC** with background mismatch calibration and noise-reduction techniques for portable medical ultrasound …

Y Liang, C Li, S Liu, Z Zhu - IEEE Transactions on Biomedical …, 2022 - ieeexplore.ieee.org

… **SAR ADC** in 65-nm CMOS technology for portable medical ultrasound systems. To break the limitation of the **ADC** linearity on the DAC size in a **SAR ADC**… generator for the **ADC** core, is …

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A 13-bit ENOB third-order noise-shaping **SAR ADC** employing hybrid error control structure and LMS-based foreground digital calibration

Q Zhang, N Ning, Z Zhang, J Li, K Wu… - IEEE Journal of Solid …, 2022 - ieeexplore.ieee.org

… This article reported a third-order NS-**SAR ADC** that leverages a hybrid error control scheme… NS-**SAR ADC**. Therefore, the proposed overall architecture is very simple and robust. …

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A 10.1-ENOB, 6.2-fJ/conv.-step, 500-MS/s, ringamp-based pipelined-**sar ADC** with background calibration and dynamic reference regulation in 16-nm CMOS

J Lagos, N Markulić, B Hershberg… - IEEE Journal of Solid …, 2022 - ieeexplore.ieee.org

… Whereas recent ringamp-based pipelined **ADCs** rank at the forefront of the per-channel speed … In this work, we present a pipelined-**SAR ADC** (see Fig. 1) that exploits ring amplification …

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A 7.3-μ W 13-ENOB 98-dB SFDR Noise-Shaping **SAR ADC** With Duty-Cycled Amplifier and Mismatch Error Shaping

H Li, Y Shen, H Xin, E Cantatore… - IEEE Journal of Solid …, 2022 - ieeexplore.ieee.org

… architecture of **SAR ADC** and **ADC**, the NS-**SAR ADC** inherits … the frontier of **ADC** performance in recent literature [1], [2]. … prior NS-**SAR ADC** designs in terms of their power efficiency. …

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Randomized switching **SAR** (RS-**SAR**) **ADC** protections for power and electromagnetic side channel security

M Ashok, EV Levine… - 2022 IEEE Custom …, 2022 - ieeexplore.ieee.org

… In this work, we propose a **SAR ADC** design (Fig. 1, 2) with Space-Time Randomization of … over an unprotected **ADC**. This work uses an 8-bit differential **SAR ADC** topology to show the …

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A fully dynamic low-power wideband time-interleaved noise-shaping **SAR ADC**

H Zhuang, J Liu, H Tang, X Peng… - IEEE Journal of Solid …, 2021 - ieeexplore.ieee.org

… This asynchronous scheme is different from a classic asynchronous **SAR ADC**, where the … The classic asynchronous **SAR ADC** suffers from an ineffective acceleration because it …

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A 625kHz-BW, 79.3 dB-SNDR second-order noise-shaping **SAR ADC** using high efficiency error-feedback structure

P Yi, Y Liang, S Liu, N Xu, L Fang… - IEEE Transactions on …, 2021 - ieeexplore.ieee.org

… into the **SAR** operation, the NS-**SAR ADC** gets higher resolution than a raw **SAR ADC** by NS effect; (2… **ADC**, the **SAR ADC** structure employs mostly digital components. It simplicity in the …

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27.5 An 80MHz-BW 640MS/s Time-Interleaved Passive Noise-Shaping **SAR ADC** in 22nm FDSOI Process

CY Lin, YZ Lin, CH Tsai, CH Lu - 2021 IEEE International Solid …, 2021 - ieeexplore.ieee.org

… rate of 10 to 12b 1b/step **SAR ADCs** is ~400MS/s, and hence … The NS pipeline-**SAR ADC** [3] was introduced to overcome … a **SAR ADC**, a timeinterleaved noise-shaping **SAR** (TINS-**SAR**) …

☆ Save 99 Cite Cited by 14 Related articles

SAR ADC

Lots of ongoing activity in SAR ADCs

A second-order noise-shaping **SAR ADC** with passive integrator and tri-l voting

H Zhuang, W Guo, J Liu, H Tang, Z Zhu... - IEEE Journal of Solid ..., 2019 - ieeexplore.ieee.or

... **SAR ADC** works, this paper proposes a novel NS-**SAR** architecture. It adds only a few swit and capacitors to a standard **SAR ADC** ... prototype 9-bit NS-**SAR ADC** is fabricated in a 40-..

Save Cite Cited by 65 Related articles All 3 versions

A calibration-free time-interleaved fourth-order noise-shaping **SAR ADC**

L Jie, B Zheng, MP Flynn - IEEE Journal of Solid-State Circuits, 2019 - ieeexplore.ieee.org

... the NS-**SAR**. To increase the bandwidth of NS-**SAR ADCs** and extend their low-power advantages, this article presents a new time-interleaved NS **SAR** (TINS-**SAR**) architecture that ...

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A 10-b 600-MS/s 2-way time-interleaved SAR ADC with mean absolute deviation based background timing-skew calibration

Jeonggoo Song ; Nan Sun

2018 IEEE Custom Integrated Circuits Conference (CICC)

Year: 2018

Pages: 1 - 4

Cited by: Papers (2)

A 32 Gb/s ADC-based PAM-4 receiver with 2-bit/stage SAR ADC and partially-unrolled DFE

Shiva Kiran ; Shengchang Cai ; Ying Luo ; Sebastian Hoyos ; Samuel Palermo

2018 IEEE Custom Integrated Circuits Conference (CICC)

Year: 2018

Pages: 1 - 4

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An 11b 80MS/s SAR ADC With Speed-Enhanced SAR Logic and High-Linearity CDAC

Yuefeng Cao ; Yongzhen Chen ; Zhekan Ni ; Fan Ye ; Junyan Ren

2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)

Year: 2018

Pages: 18 - 21

A 24-to-72GS/s 8b time-interleaved SAR ADC with 2.0-to-3.0pJ/conversion and >30dB SNDR at nyquist in 14nm CMOS FinFET

Lukas Kull ; Danny Luu ; Christian Menolfi ; Matthias Braendli ; Pier Andrea Francese ; Thomas Morf ; Marcel Kossel ; Alessandro Cevrero ; Ilter Ozkaya ; Thomas Toifl

2018 IEEE International Solid - State Circuits Conference - (ISSCC)

Year: 2018

Pages: 358 - 360

A 12-bit 20-MS/s SAR ADC With Fast-Binary-Window DAC Switching in 180nm CMOS

Yung-Hui Chung ; Yi-Shen Lin ; Qi-Feng Zeng

2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)

Year: 2018

Pages: 34 - 37

IEEE Conferences

Abstract (html) (2687 Kb)

An 18-bit 2MS/s pipelined SAR ADC utilizing a sampling distortion cancellation circuit with −107dB THD at 100kHz

Derek Hummerston ; Peter Hurrell

2017 Symposium on VLSI Circuits

Year: 2017

Pages: C280 - C281

Cited by: Papers (2)

SAR ADC

Lots of ongoing activity in SAR ADCs

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IEEE Conferences
Abstract (html) (2687 Kb) ©

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Year: 2018
Pages: 18 - 21

A 32 Gb/s ADC-based PAM-4 receiver with 2-bit/stage SAR ADC and partially-unrolled DFE
Shiva Kiran ; Shengchang Cai ; Ying Luo ; Sebastian Hoyos ; Samuel Palermo
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Year: 2018
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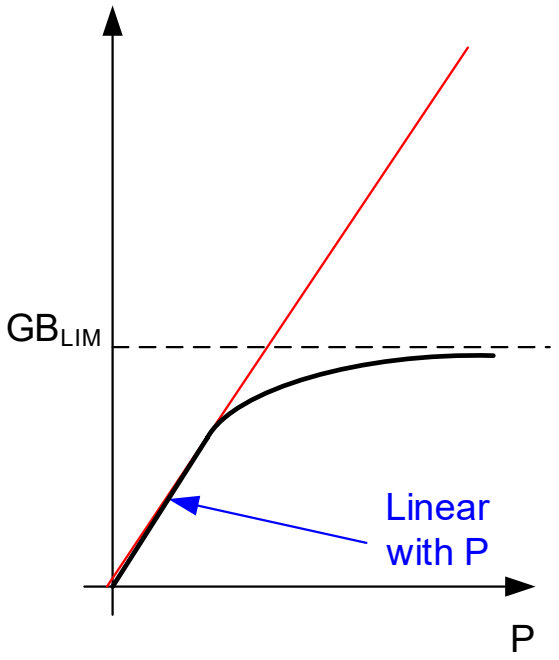
Cited by: Papers (4)

An 18-bit 2MS/s pipelined SAR ADC utilizing a sampling distortion cancellation circuit with −107dB THD at 100kHz
Derek Hummerston ; Peter Hurrell
2017 Symposium on VLSI Circuits
Year: 2017
Pages: C280 - C281
Cited by: Papers (2)

Time Interleaved ADCs

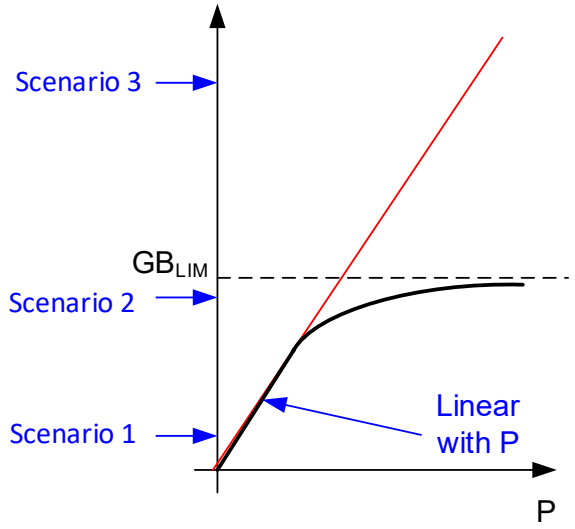
- At higher sampling rates power dissipation of ADCs becoming too high
- Some (many) product opportunities that can not be captured using existing ADC architectures in a given process

Typical tradeoffs between P and GB for Op Amps



Attributable to parasitic capacitance effects at high frequencies

Time Interleaved ADCs



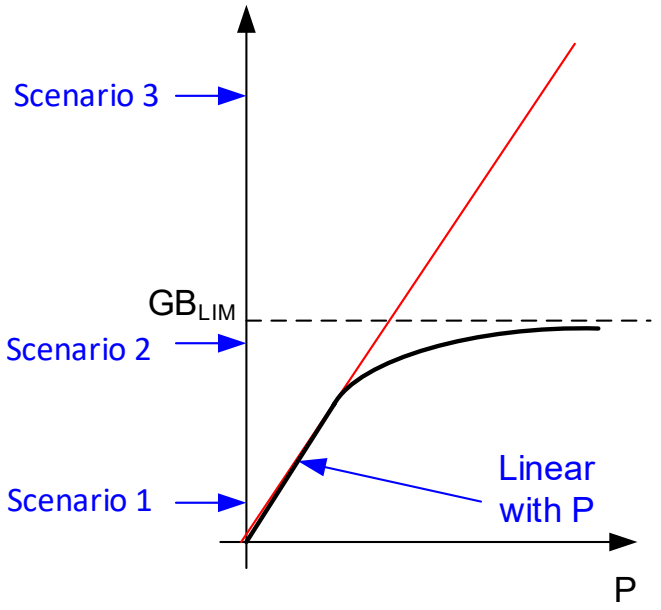
Settling time of amplifiers proportional to GB^{-1}

Operating two amplifiers with a double setting time would require same power as operating a single amplifier if operating on linear part of this curve (Scenario 1)

Operating on nonlinear part of curve has unfavorable power requirement (Scenario 2)

Technology will not support GB requirements in excess of GB_{LIM} (Scenario 3)

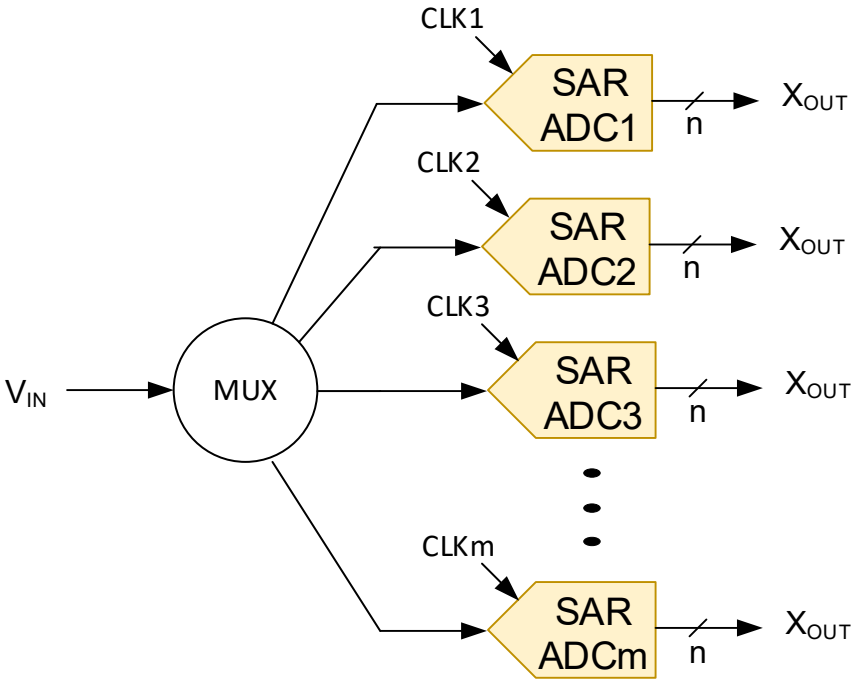
Time Interleaved ADCs



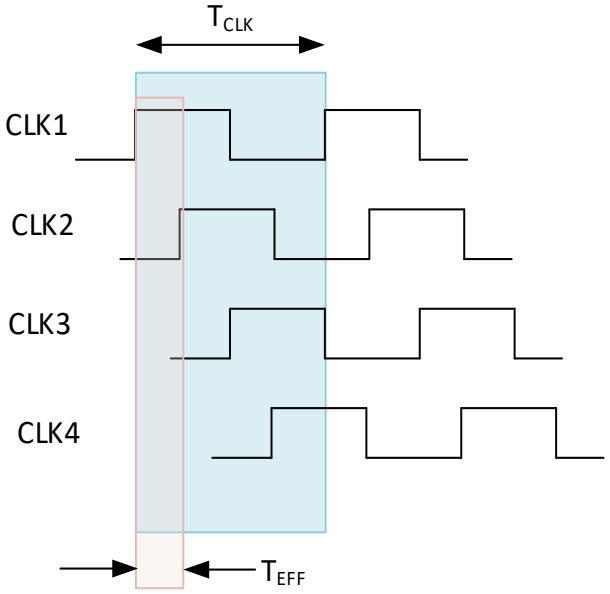
Time interleaving (if a fast S/H is available) will allow operation on the linear portion of the curve even if GB requirements for a standard solution exceed GB_{MAX} or will reduce power dissipation if standard solution forces operation on the nonlinear portion of the curve.

Though interleaving of either pipelined ADCs or SAR ADCs is possible, interleaving of SAR ADCs is getting lots of attention

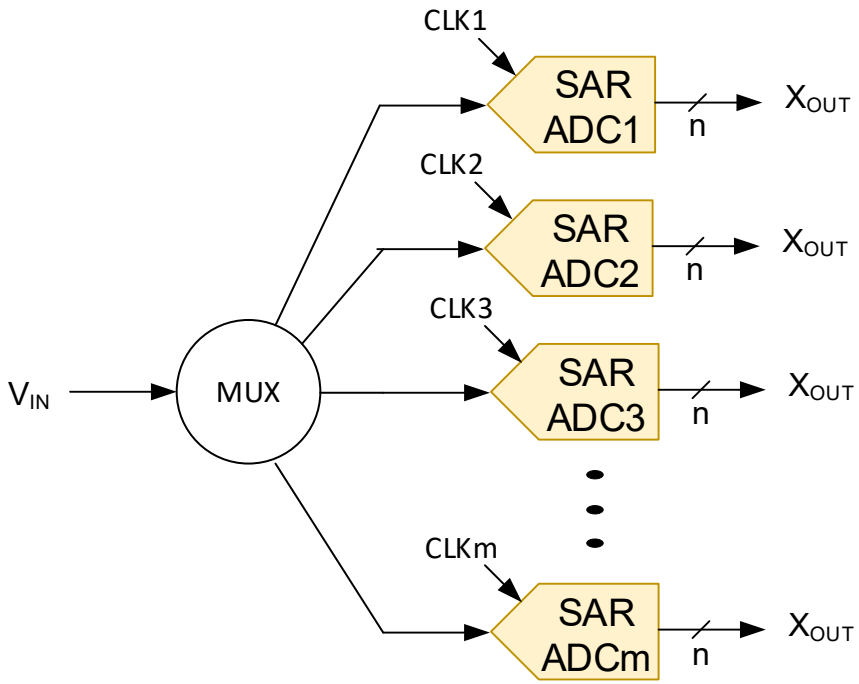
Time Interleaved SAR ADC



Time interleaving increases effective conversion rate by factor of m

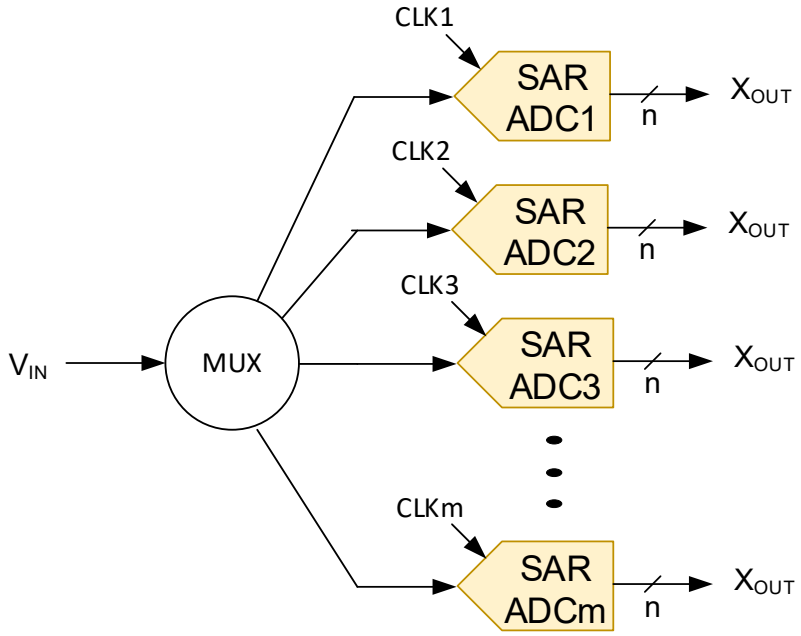


Time Interleaved SAR ADC



- Provides high-speed solution when single SAR can not operate fast enough
- May be more energy efficient even is single SAR can work
- May provide better performance than pipelined structure
- Matching between stages is critical
- Clock phasing is critical
- Calibration is essential to provide matching and phasing

Time Interleaved SAR ADC



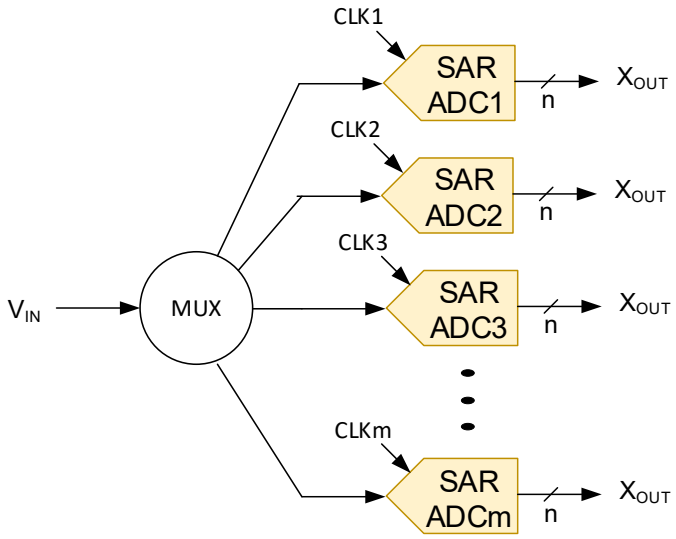
Idea is 40+ years old but only recently has become popular

Though idea was straightforward, challenges of practical implementations were considered impractical for many years

W. Black and D. Hodges, “Time Interleaved Converter Arrays,” IEEE J. Solid-State Circuits, Dec. 1980, pp. 1022–29. 1081 citations (May 3, 2023)

Four 7-bit Charge Redistribution SAR ADCs

Time Interleaved SAR ADC



The challenges:

1. Offset missmatch
2. Gain mismatch
3. Timing skew
4. Bandwidth Missmatch
5. Nonlinearity Missmatch
6. Front-end fast S/H

Time Interleaved SAR ADC

Good Reference:

https://www.analog.com/media/en/technical-documentation/tech-articles/The-ABCs-of-Interleaved-ADCs.pdf

Time Interleaved SAR ADC

The ABCs of Interleaved ADCs

Jonathan Harris, Applications Engineer

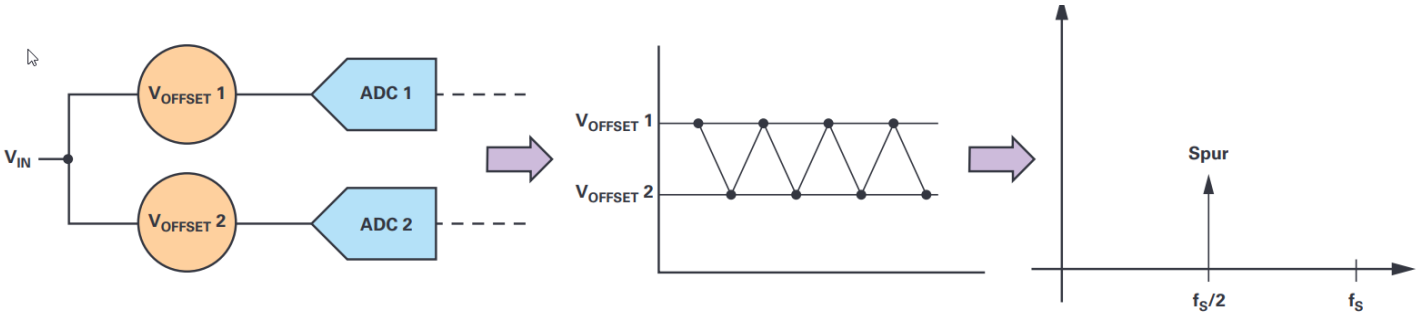


Figure 4. Offset mismatch.

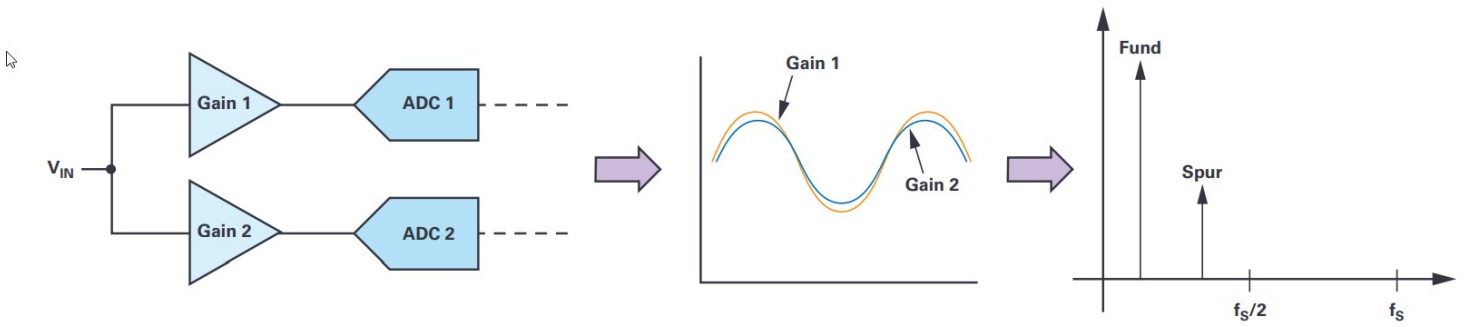


Figure 5. Gain mismatch.

Time Interleaved SAR ADC

The ABCs of Interleaved ADCs

Jonathan Harris, Applications Engineer

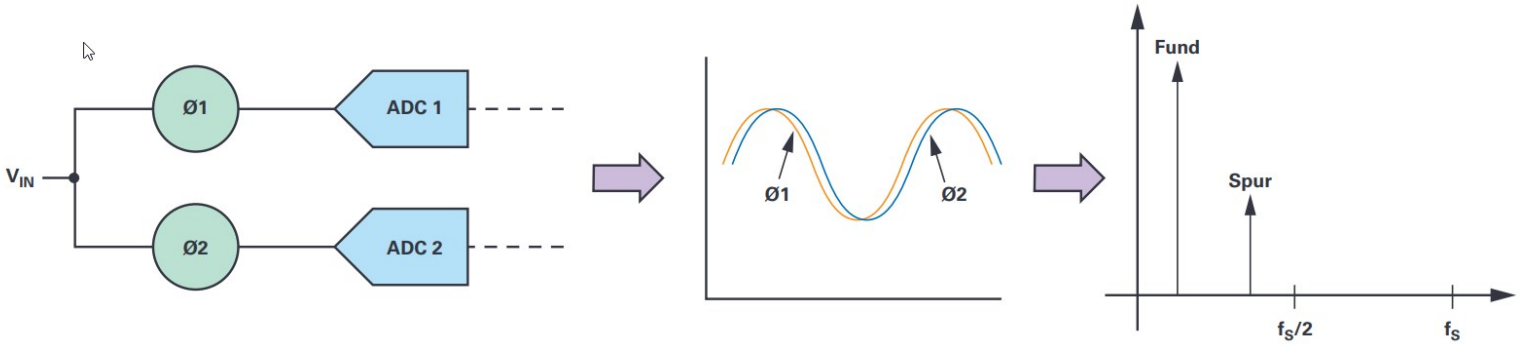


Figure 6. Timing mismatch.

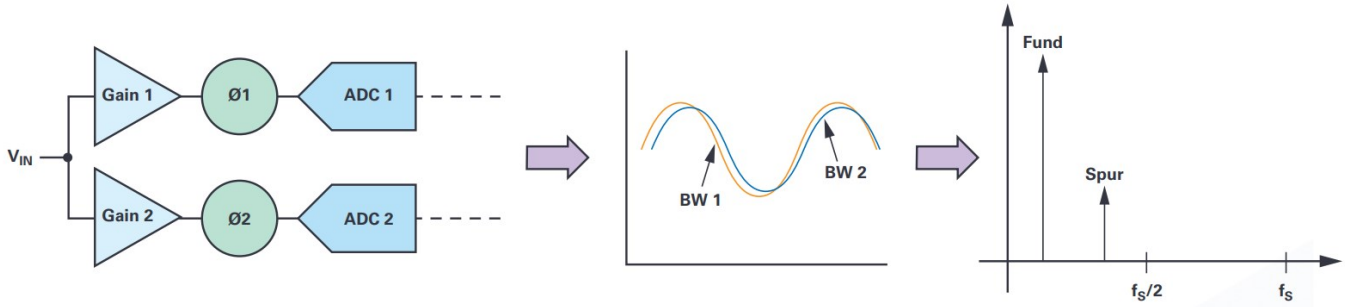
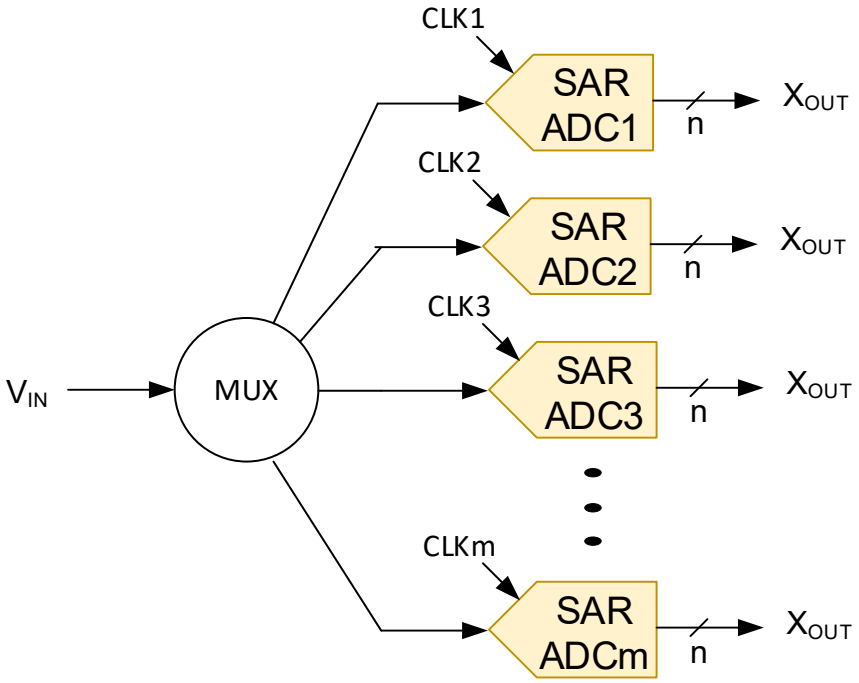


Figure 7. Bandwidth mismatch.

Time Interleaved SAR ADC



- Provides high-speed solution when single SAR can not operate fast enough
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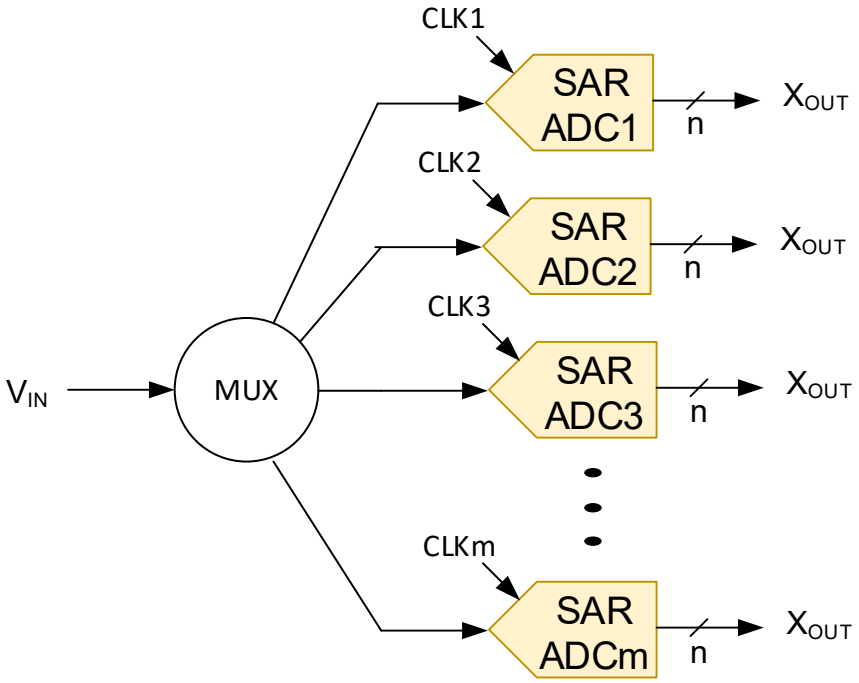
- Calibration is essential to provide matching and phasing

Time Interleaved SAR ADC

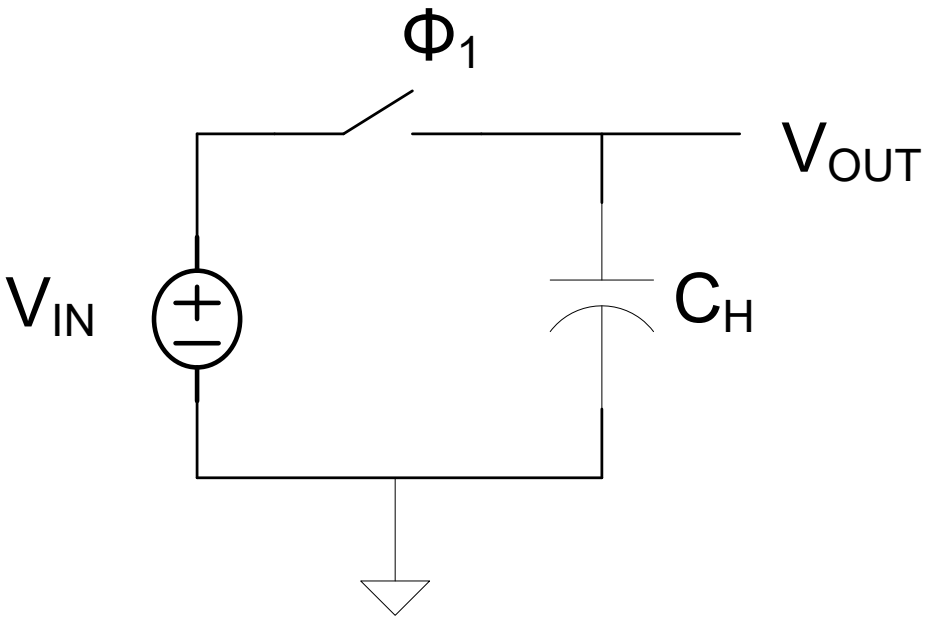


Time Interleaved ADCs are becoming very popular

Considerable interest in research community and in industry !

Bootstrapped Switch

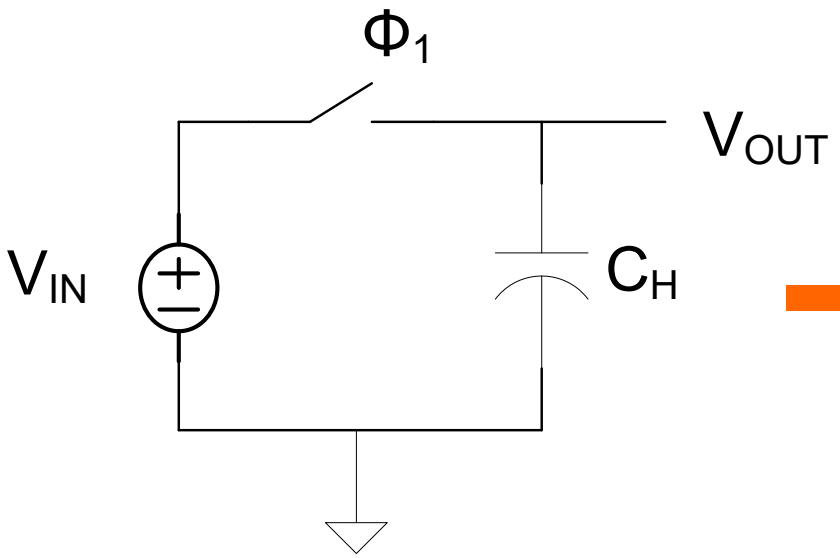
The ideal sampling operation



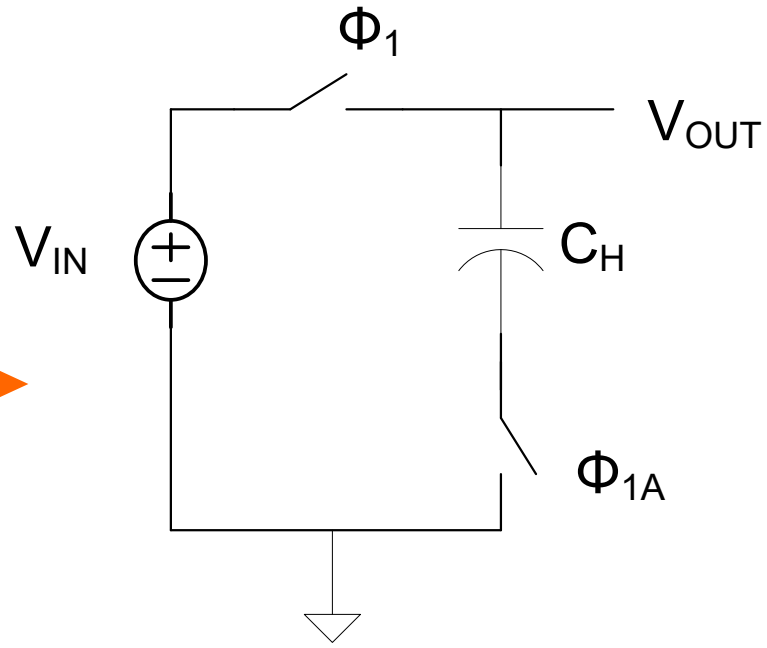
Should track V_{IN} in the TRACK mode
Should accurately sample V_{IN} at transition to HOLD mode

Bootstrapped Switch

The ideal sampling operation



Single V_{IN}-referenced switch

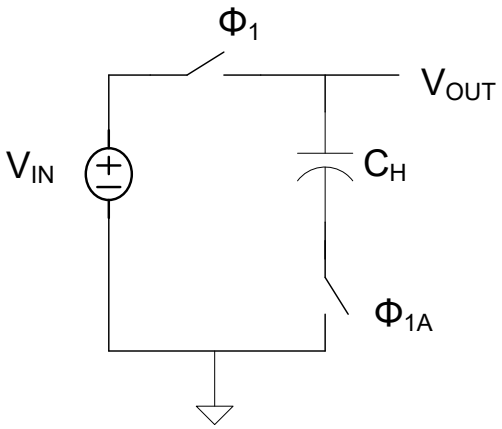


Bottom plate sampling

Should track V_{IN} in the TRACK mode
Should accurately sample V_{IN} at transition to HOLD mode

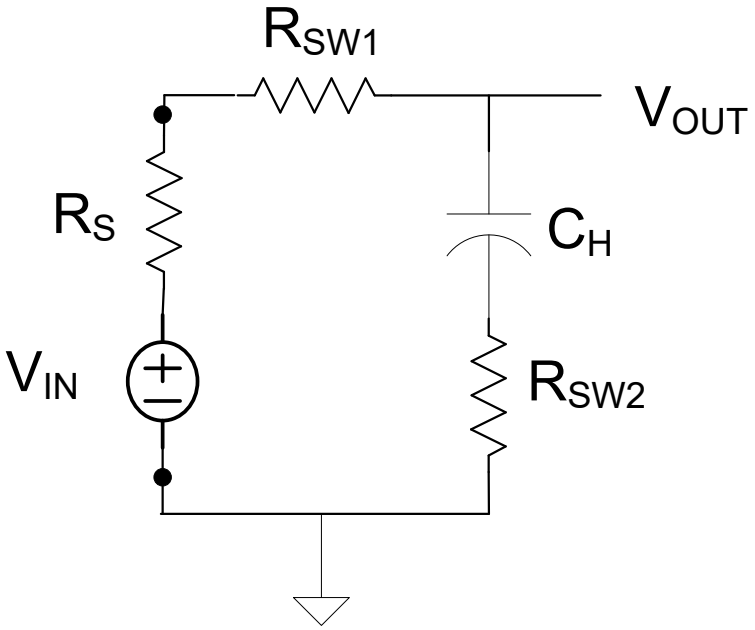
Bootstrapped Switch

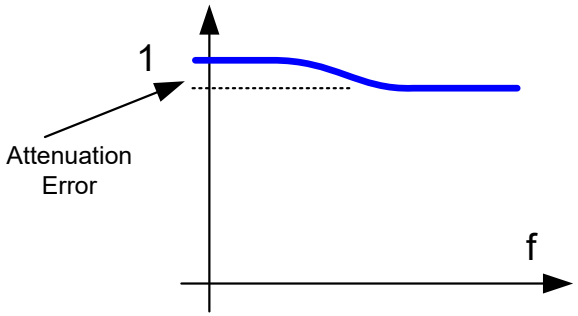
The ideal sampling operation



$$\frac{V_{OUT}}{V_{IN}} = \frac{1+R_{SW2}C_L s}{1+(R_S+R_{SW1}+R_{SW2})C_L s}$$

If linear





For high frequency inputs, an attenuation error will occur

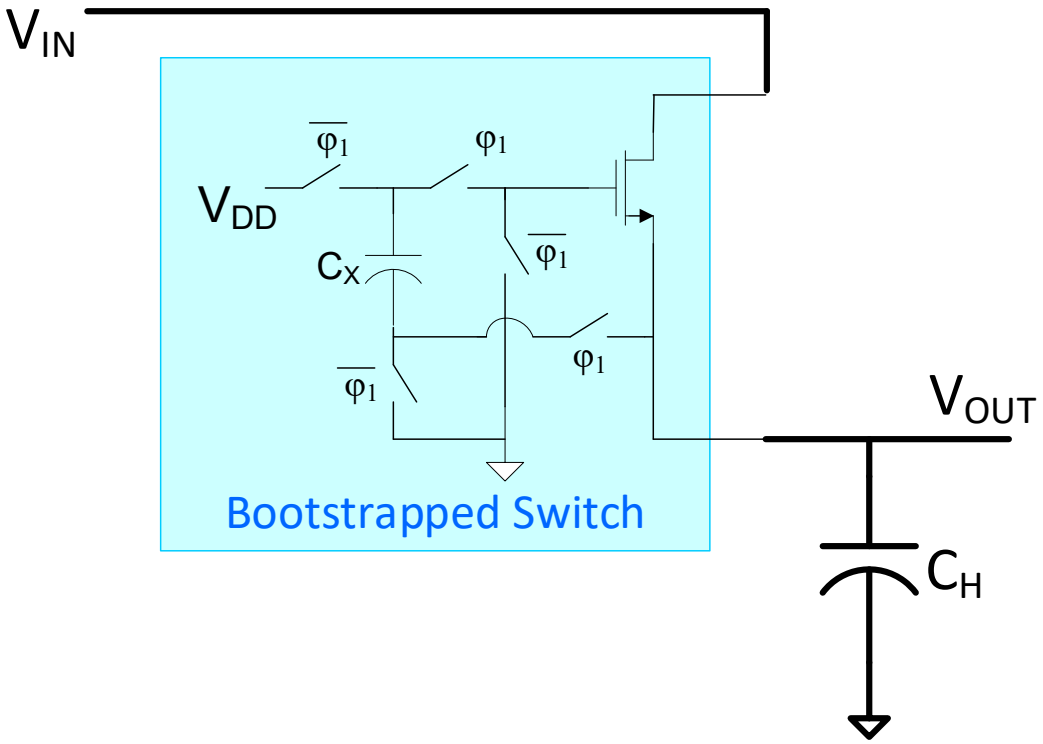
Affects absolute accuracy but not linearity (if switches linear)

But, if switches are nonlinear, will introduce a nonlinear error that can be very substantial

Signal dependent R_{SW} or switch nonlinearity will introduce nonlinear errors

Bootstrapped Switch

Bootstrapping Principle



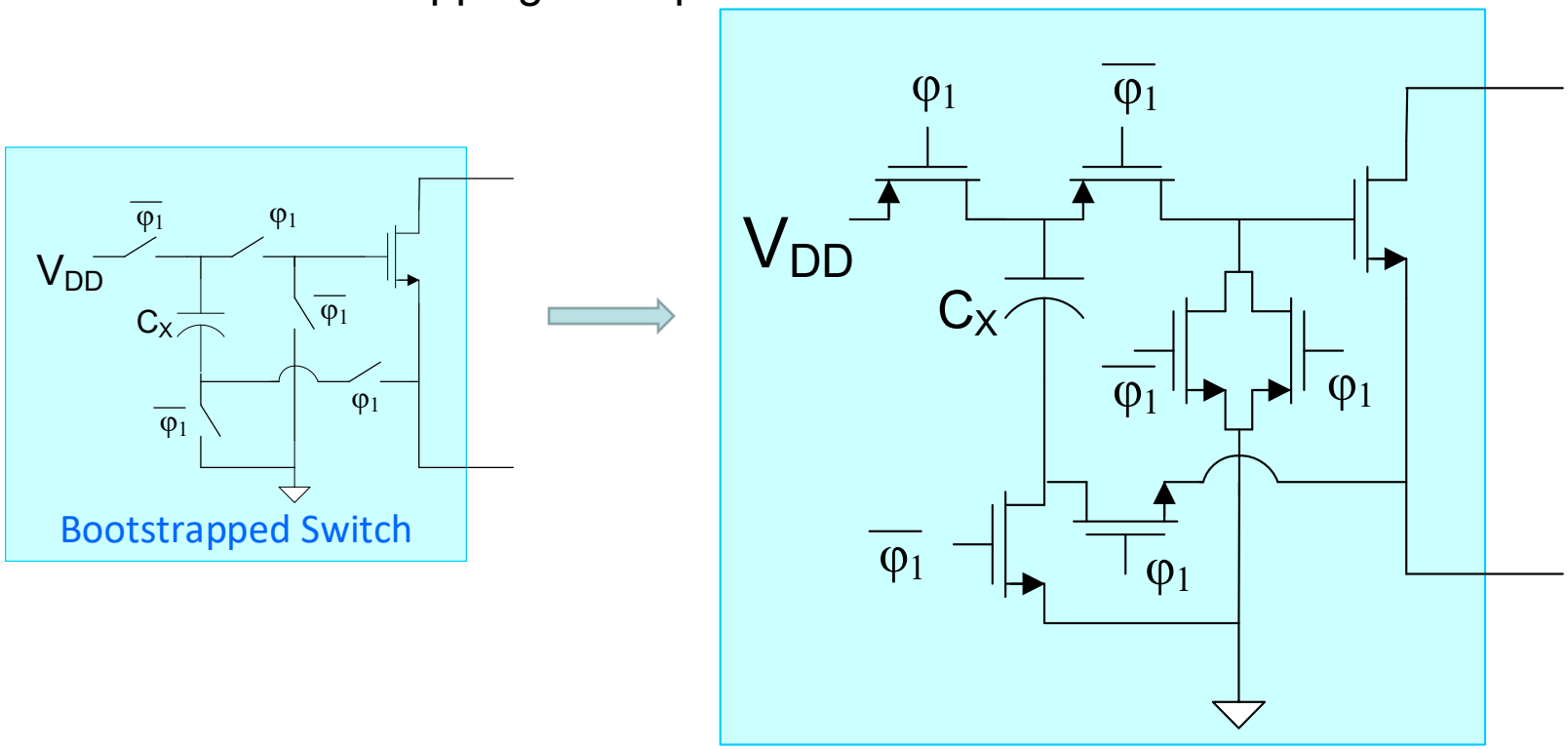
During phase $\overline{\phi}_1$ C_X is charged to V_{DD} and MOS switch is OFF

During phase ϕ_1 C_X is placed across V_{GS} and MOS switch is ON

With bootstrapping, R_{SW} is independent of V_{IN}

Bootstrapped Switch

Bootstrapping Principle

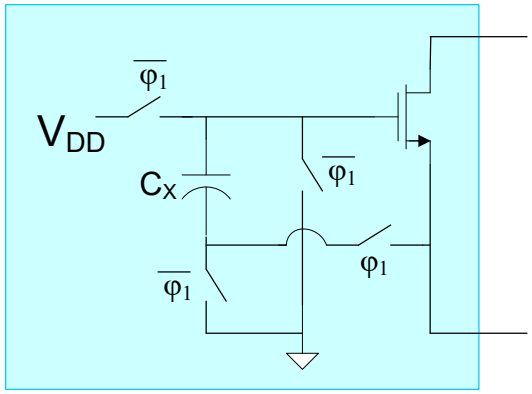


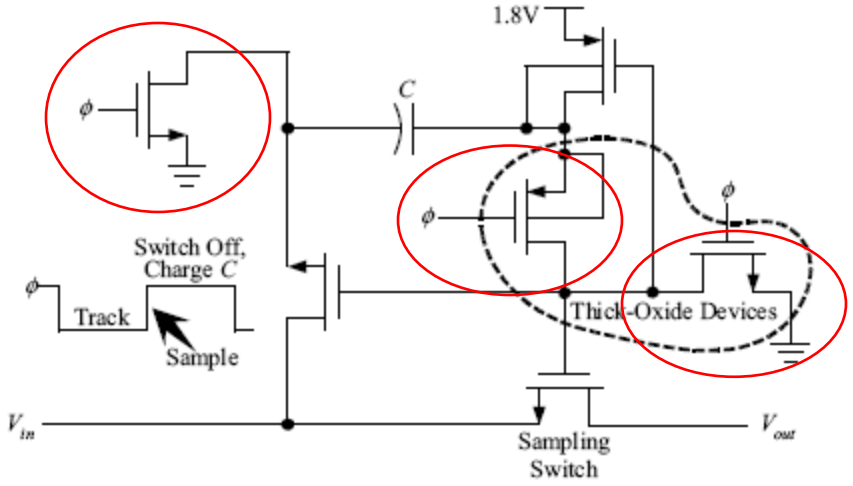
Conceptual Realization

- May have difficult time turning on some switches
- May stress gate oxide !

Bootstrapped Switch

Bootstrapping Principle



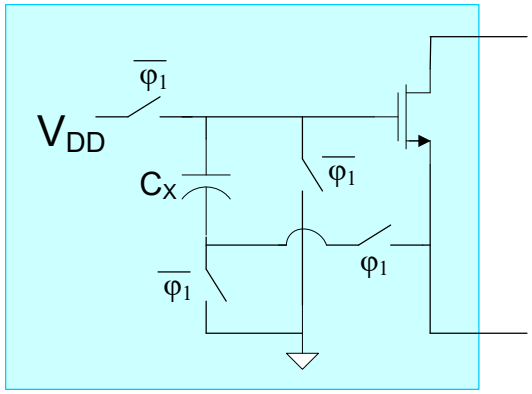


From Galton, ISSCC 04

Note: Signal does not affect turn-on time or voltage of sampling switches (all relative to VDD or GND)

Bootstrapped Switch

Bootstrapping Principle



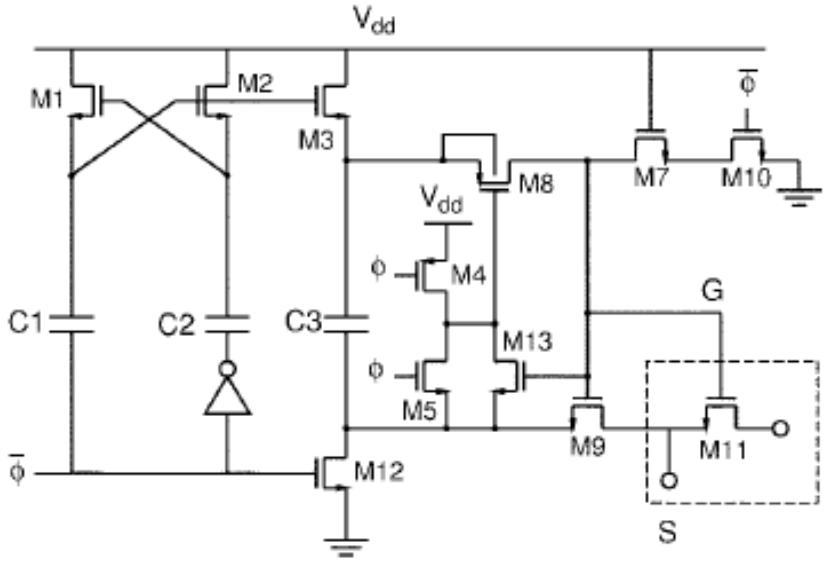
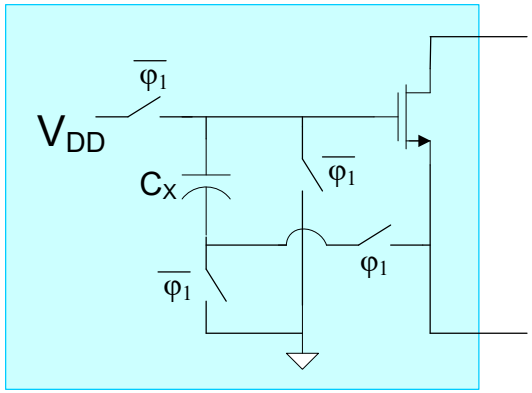


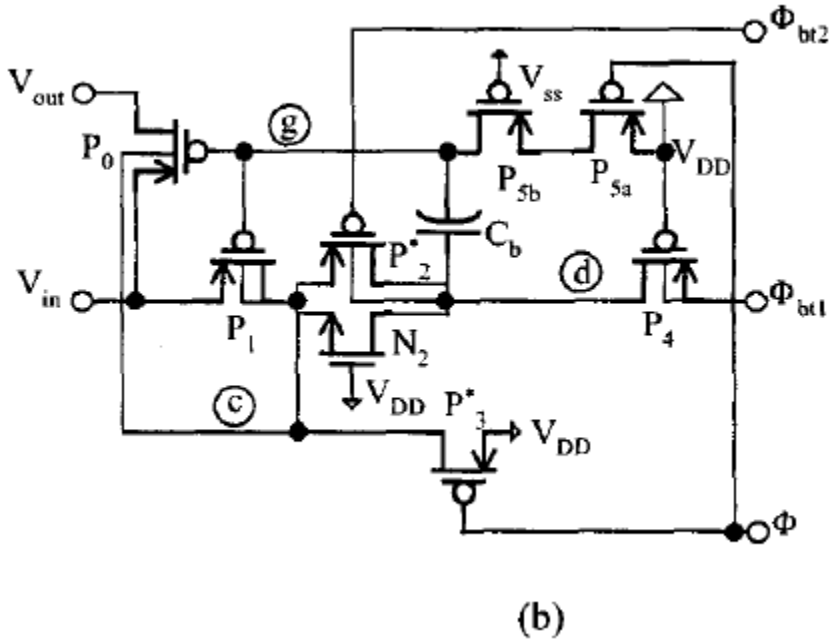
Fig. 7. Bootstrap circuit and switching device.

From Abo and Gray JSC 99

Bootstrapped Switch

Bootstrapping Principle



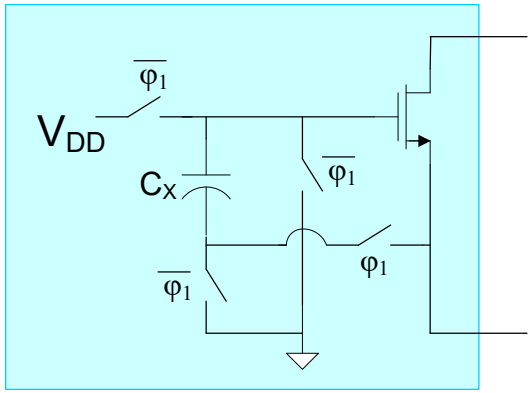


(b)

From Roberts MWSCAS 2000

Bootstrapped Switch

Bootstrapping Principle



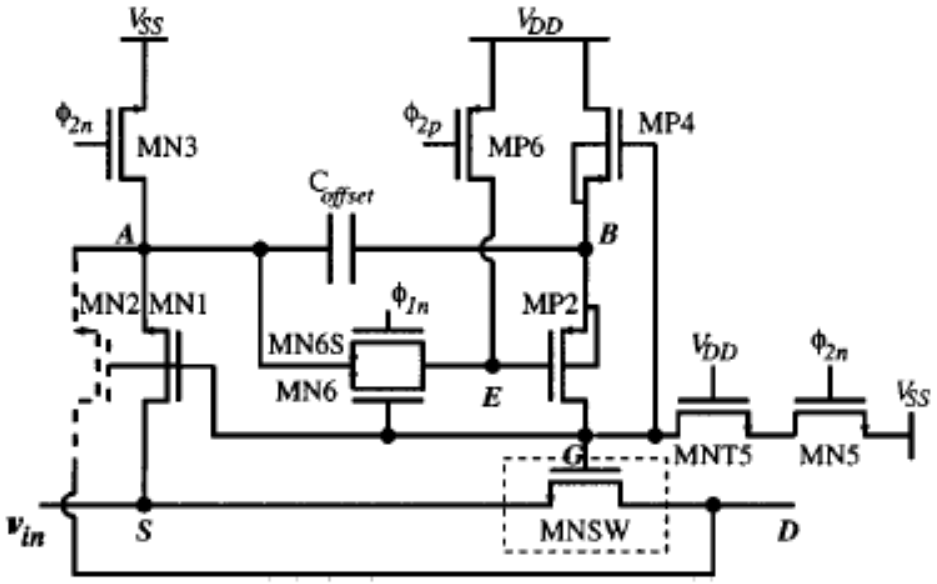
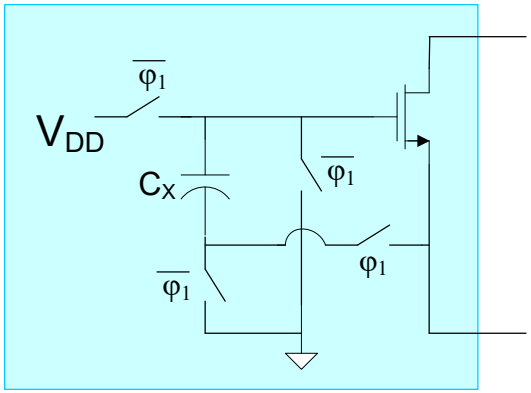


Fig. 7. Transistor-level implementation of the bootstrapped switch.

From Kaiser JSC 2001

Bootstrapped Switch

Bootstrappi



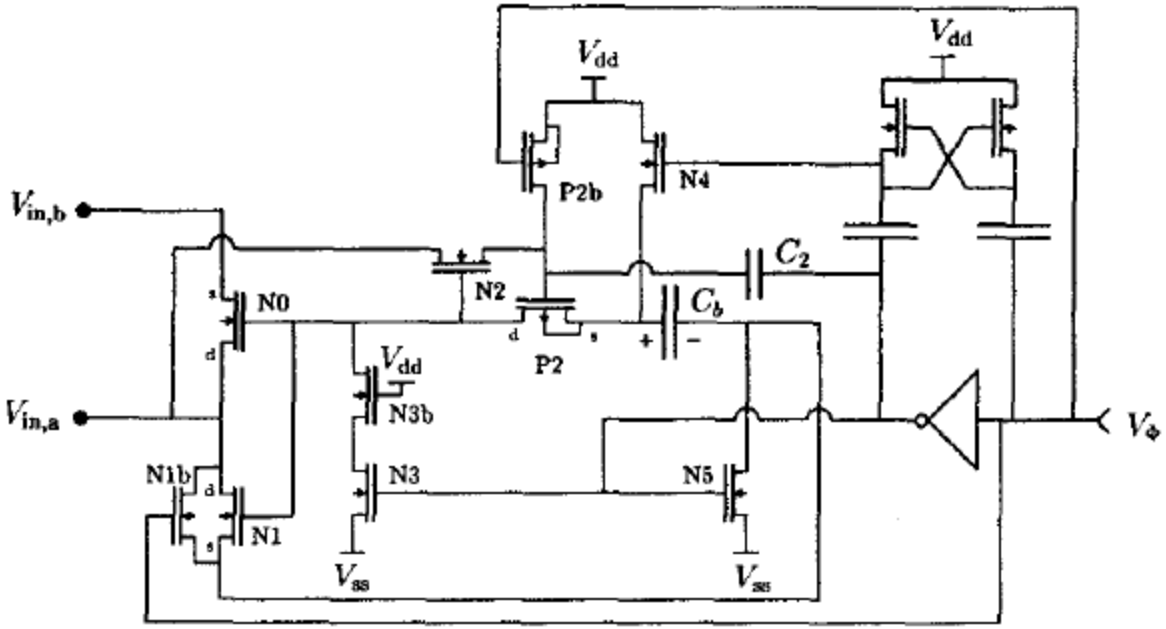


Figure 5: Bootstrapped switch.

From Steensgaard ISCAS 1999

Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Op Amp Gain causes finite gain errors and introduces noninearity	2. a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3. Op amp settling must can cause errors	3. Select GB to meet settling requirements (degrade modestly to account for slewing)
4. Power dissipation strongly dependent upon GB of Op Amps	4. Minimize C_L, use energy efficient op amps, share or shut down op amp when not used,scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies. Good (near optimal) noise distribution strategy should be followed.
5. Choice of FB Amplifier Architecture seriously impacts performance	5. Bottom plate sampling, bootatrapping, clock advance to reduce aperature uncertainty,critical GB, parasitic insensitivity needed, β dependent upon architecture and phase, compensation for worst-case β, TG if needed
6. Correct interpretation of α_k's is critical	6. a) Accurately set α_k values b) Use analog or digital calibration

Pipelined Data Converter Design Guidelines

	Issue	Strategy
7.	Sampling operation inherently introduces a sampled-noise due to noise in resistors	Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage) .
8.	Signal-dependent tracking errors at input introduce linearity degradation	Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches

Stay Safe and Stay Healthy !

End of Lecture 26